TINA

PCB Design Manual

DesignSoft

www.designsoftware.com

CREATING A PRINTED CIRCUIT BOARD (PCB)

Using TINA 7, you've captured the schematic of your circuit and refined the design. It's time to make a prototype of the circuit or to manufacture it. It's good to know that you can continue the process still using TINA 7 Design Suite (and later versions), since PCB design is now an integral part of the program.

Let's learn how to design a PCB by working through a few examples.

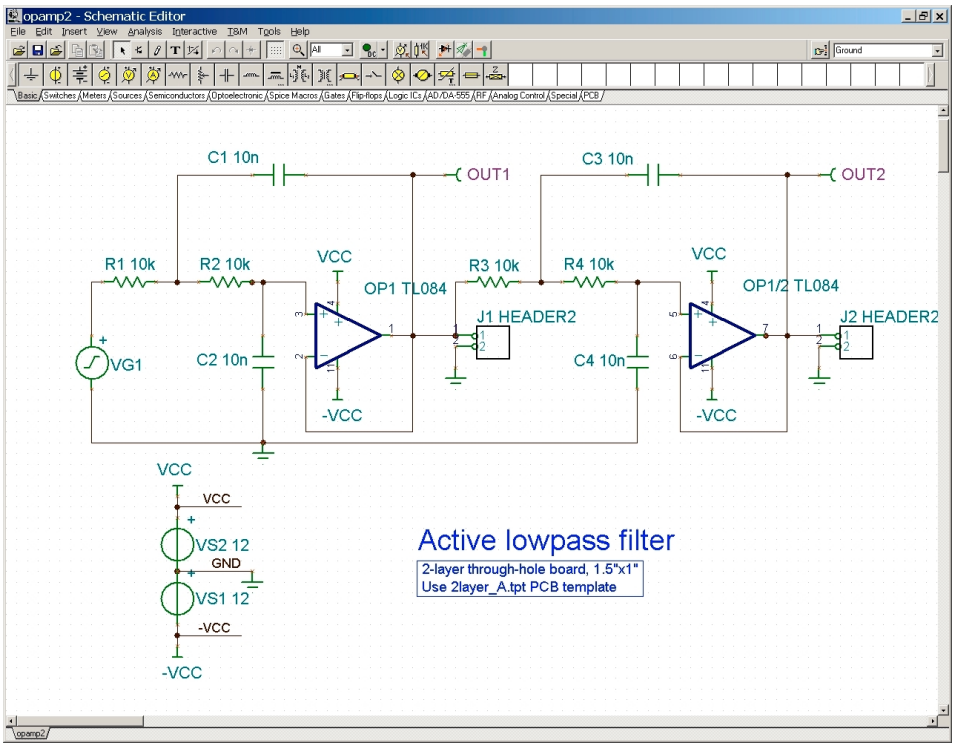
Note that the different phases of the presented design examples have been saved in the TINA's Examples/PCB directory using the following naming conventions:

*** origin.tsc**	original schematic file
***.tsc**	backannotated schematic file (after pin/gate swapping)renumbering)
*** placed.tpc**	design parameters set, components placed pcb file
*** routed.tpc**	net properties set and routed pcb file
*** finished.tpc**	optionally pin/gate swapped and renumbered, routed, silkscreen adjusted, documentation layers finalized pcb file

If you save your versions of these demo examples, be careful not to overwrite the original files TINA installed.

1.1 Setting and checking footprint names

As a first example, open the opamp2.tsc project from TINA's Examples/PCB folder. The following schematic will appear:



To achieve an accurate PCB design, one that is easy to build, every part in your schematic must have a physical representation with exact physical size. This is realized through so-called footprints: drawings showing the outline and the pins of the parts.
The footprint naming convention in TINA Pro uses as a starting point the IPC-SM-782A (Surface Mount Design and Land Pattern Standard) and the JEDEC standard JESD30C (Descriptive Designation System for Semiconductor-Device Packages, see http://www.jedec.org/download/search/jesd30c.pdf.). However, the libraries do not conform to any given set of industry or manufacturer standards because standards have difficulty keeping up to date when technology changes faster than the standards. Generally, standards mirror a fixed set of data at a point in time, while new manufacturing capabilities lead to ever-smaller new footprints with more and more pins.

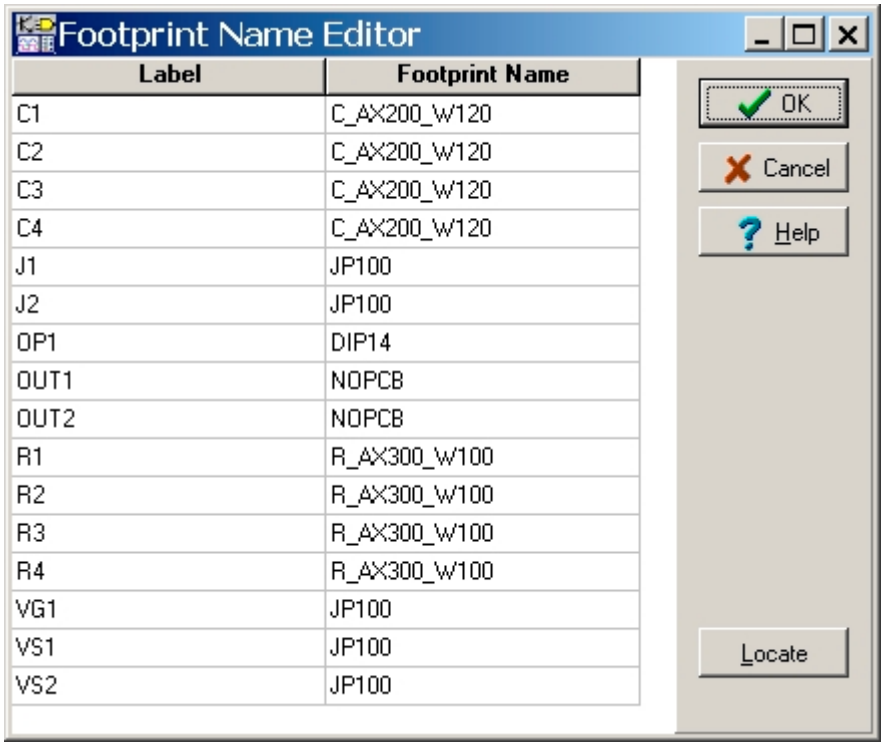
We have already assigned default footprint names to all parts that represent real components.

Note that some parts used for theoretical investigations, controlled sources, for example, do not represent real physical parts and cannot be placed on a PCB. If your desig contains such components, you should replace them with real physical parts.

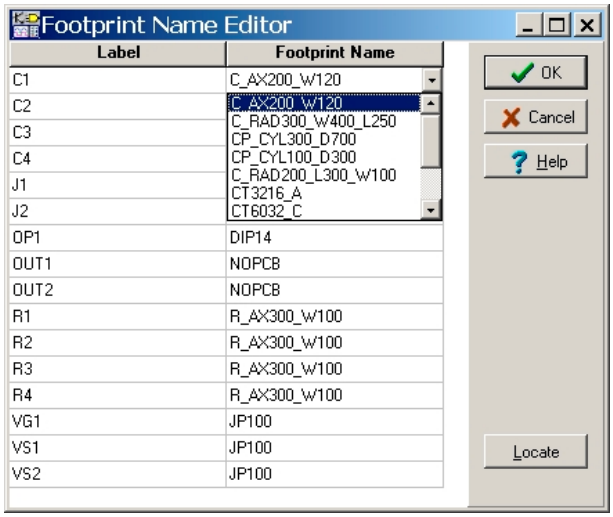
Of course there is no guarantee that the default physical packages of TINA's parts are the same as needed by your design.

There are two ways to check this.

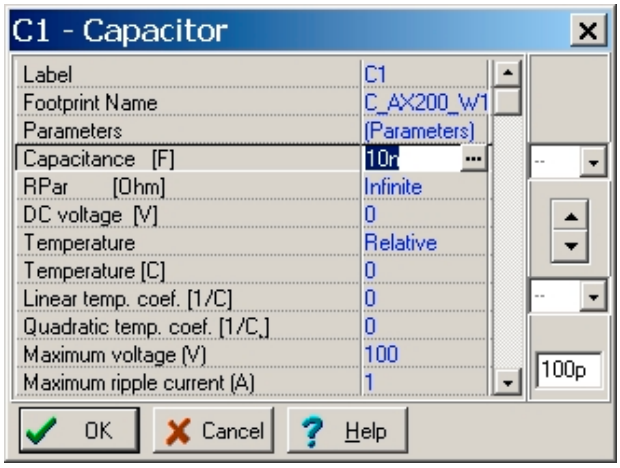
1) You can use TINA's "Footprint name editor", which you can invoke from TINA's Tools menu. In this dialog you can see all of TINA's components and their corresponding footprint names.



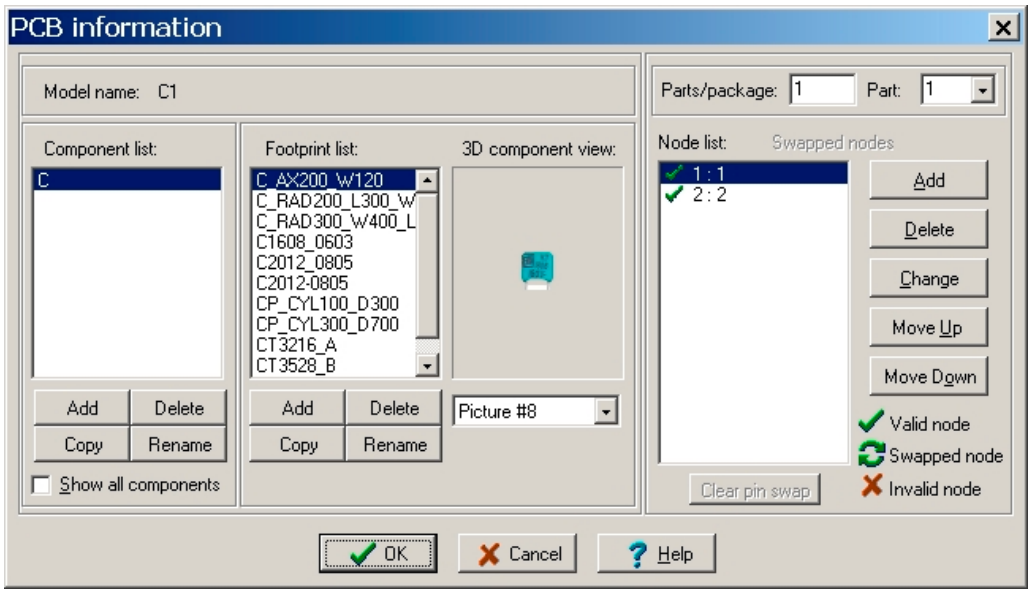
Select from the available footprint names by clicking on the footprint name fields. In the dialog box, components with no footprint name association are denoted by red characters and by "???" in the footprint name field.



2) The second way to examine the assigned footprints is to double-click on each part and check the Footprint Name in the component property dialog that appears.



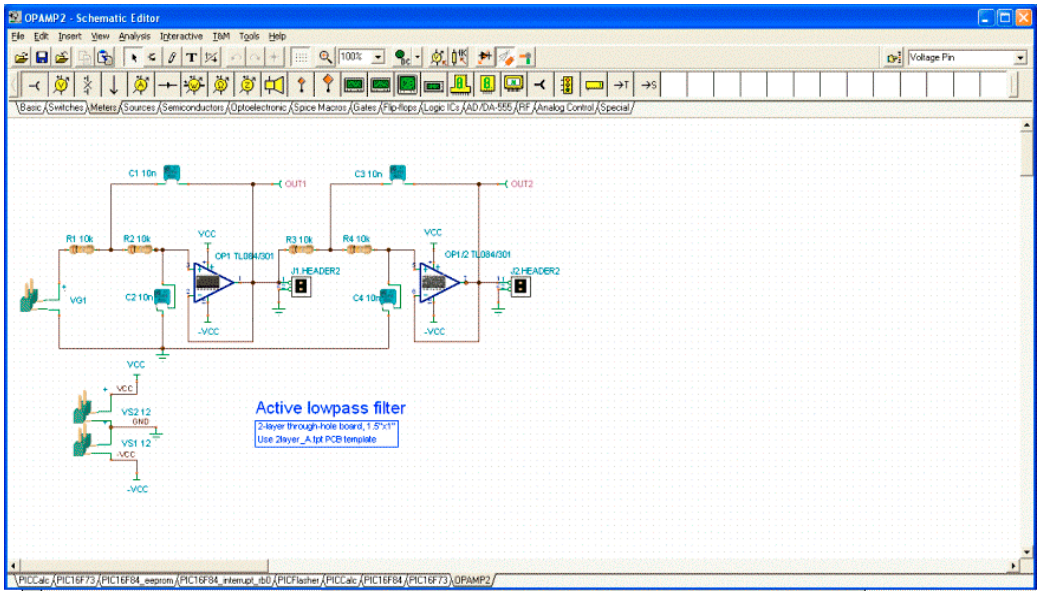
You can also click the ... button in the Footprint Name line to invoke the "PCB information" dialog. This allows you to select from the available footprint names on the Footprint list. Here you can also find and display the 3D view of the parts on the list.



When you find the footprint you seek, click on it and press OK. This will return you to the component property dialog with the selected footprint name in the Footprint name line. To confirm the change, press OK on the component property dialog again.

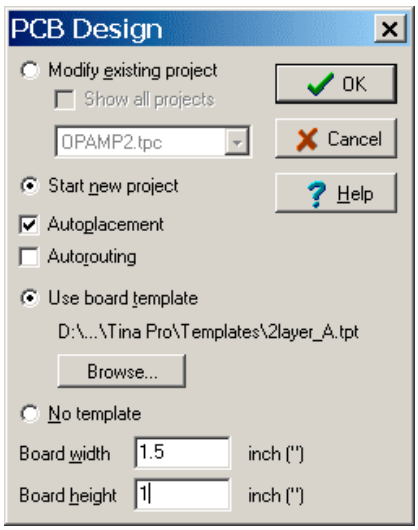
If you don't find the footprint you want, you can create a new one. Start by pressing the Add button of the "PCB information" dialog. Of course, it's not enough to just add a footprint name in this dialog–you must also add the corresponding footprint to PCB's footprint library. For details, see chapter 6 – Making your own schematic symbols and footprints – of the Quick Start Manual.

When you're done, check the 2D/3D shape by clicking the 2D/3D view button or the F6 key. Unless a component is only meaningful for analysis, it will have a 3D view. If the physical part association is OK, we can begin the PCB layout design.



1.2 Invoking TINA PCB

To begin PCB design, press the button on TINA's toolbar (the last one o the right) or select the "PCB Design" command on the Tools menu. Set the parameters as shown below.



Select "Start New Project," "Autoplacement," and "Use board template." With th Browse button find and select the 2layer_A.tpt template file from TINA's Template folder. Using this file will ensure the proper settings for a double-sided PCB.

When starting with a TINA template, you are choosing the level of manufacturing complexity of your project. The following three levels of manufacturing technology are defined by the IPC-2221 generic standard:

Level A : General Design Complexity
Level B : Moderate Design Complexity
Level C : High Design Complexity

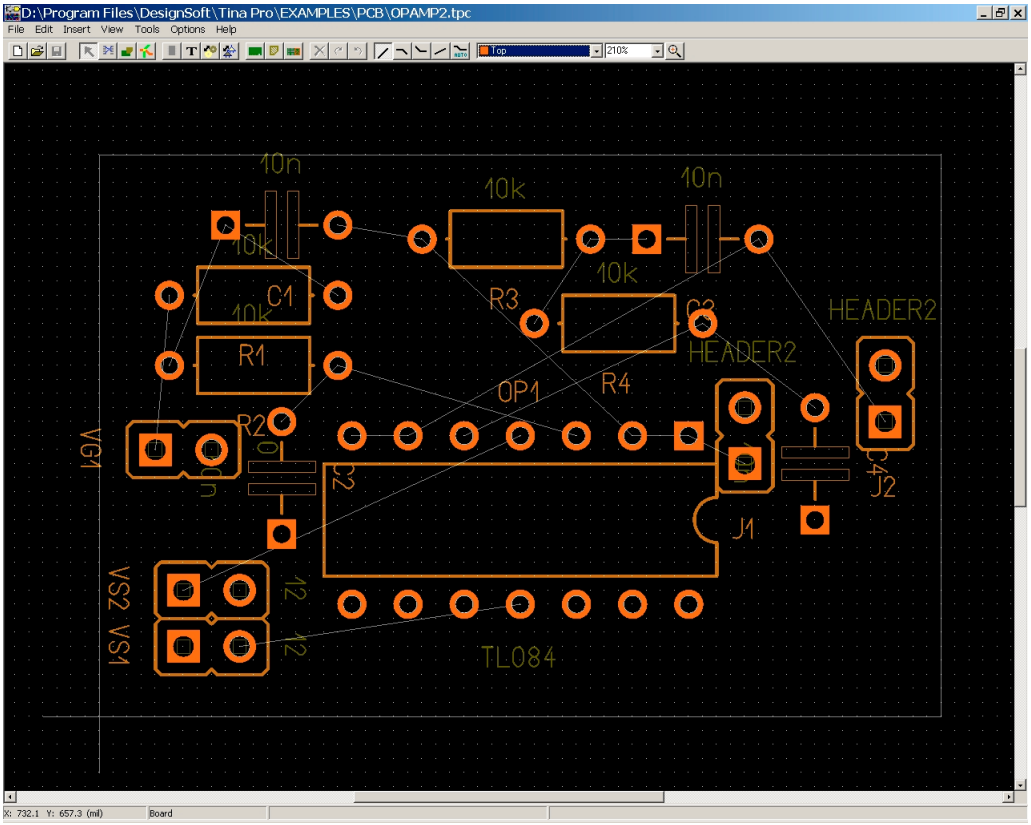
The template file specifies the number of layers, including their properties, system grid size, autorouter settings, spacing and track width. The following templates are included with PCB Designer:

	Level	Routing Layers	Plane Layers	Routing	Spacing	Comments
1layer_A.tpt	A	1	-	25	12 1/2	Allows one track between standard IP IC pin
2layer_A.tpt	A	2	-	25	12 ½	
2layer_B.tpt	B	2	-	8 1/3	8 1/3	Use for SMT or mixed-technoly board
2layer_B_mm.tpt	B	2	-	0.1	0.2	
4layer_C_mm.tpt	C	2	2	0.1	0.15	For moderate and high density

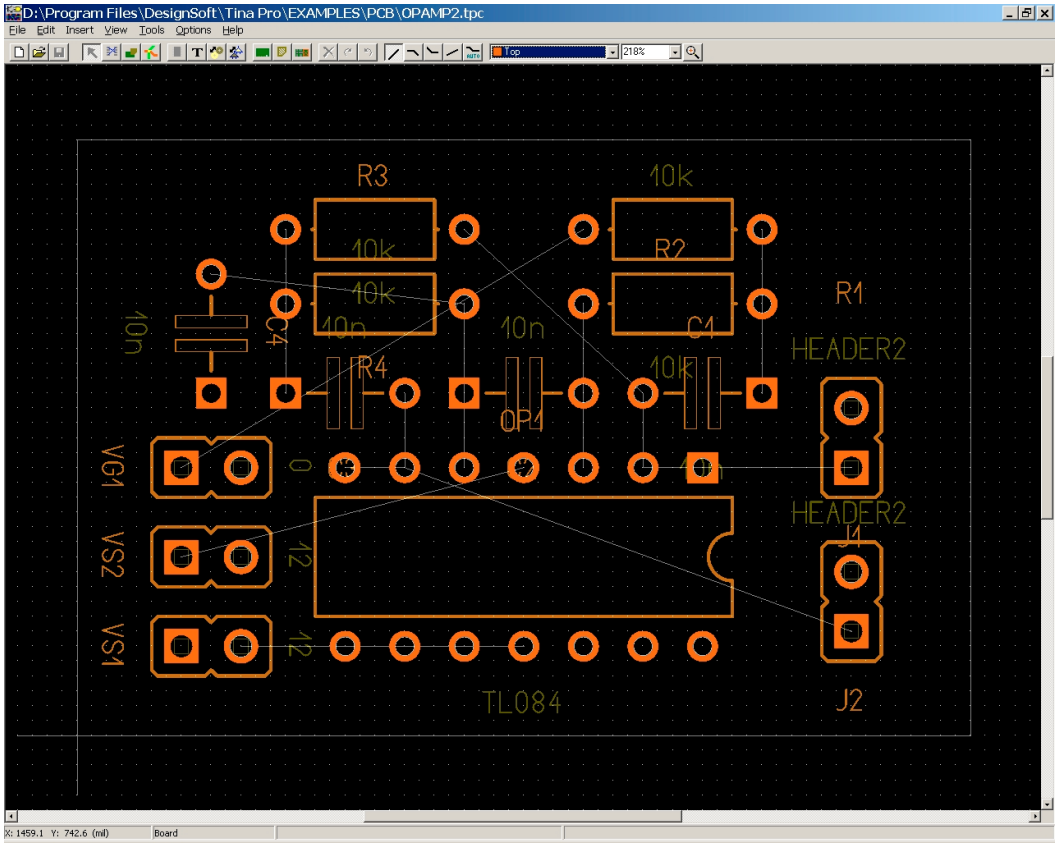
In choosing a PCB template, you should take into consideration technology, density, and package pitch.

To complete the set up, set the PCB size in inches or mm depending on the measurement unit settings in the View/Options dialog of TINA.

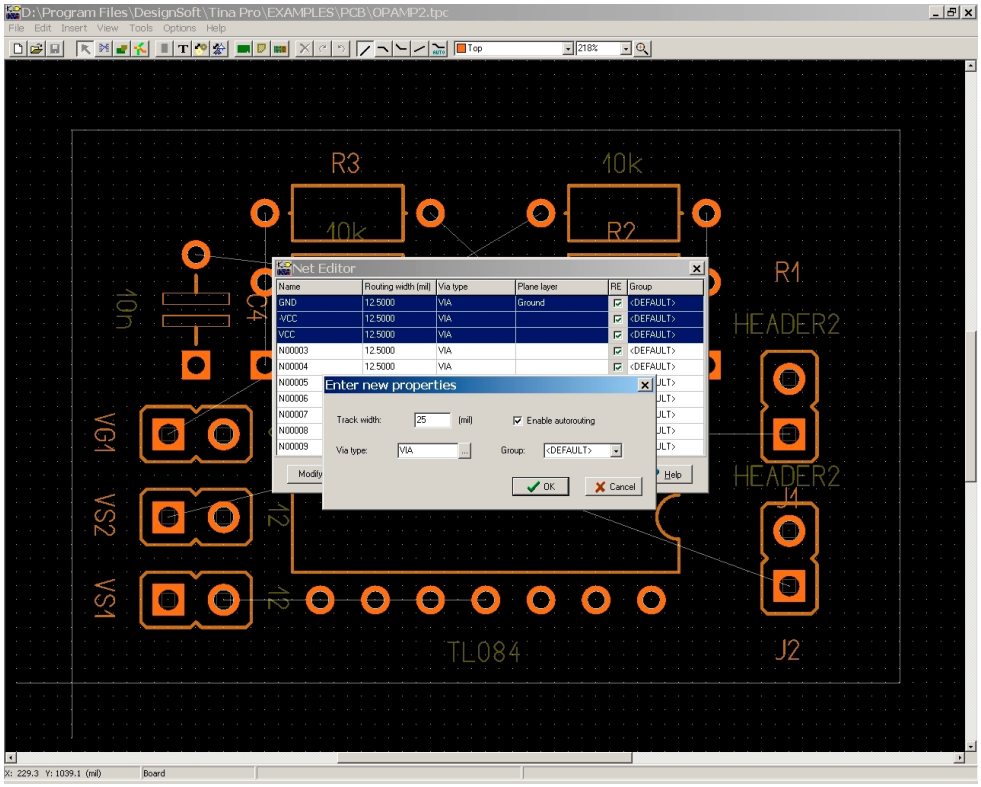
Now that everything is set properly press the OK button and the PCB layout design will appear with all the components automatically placed on the PCB board.



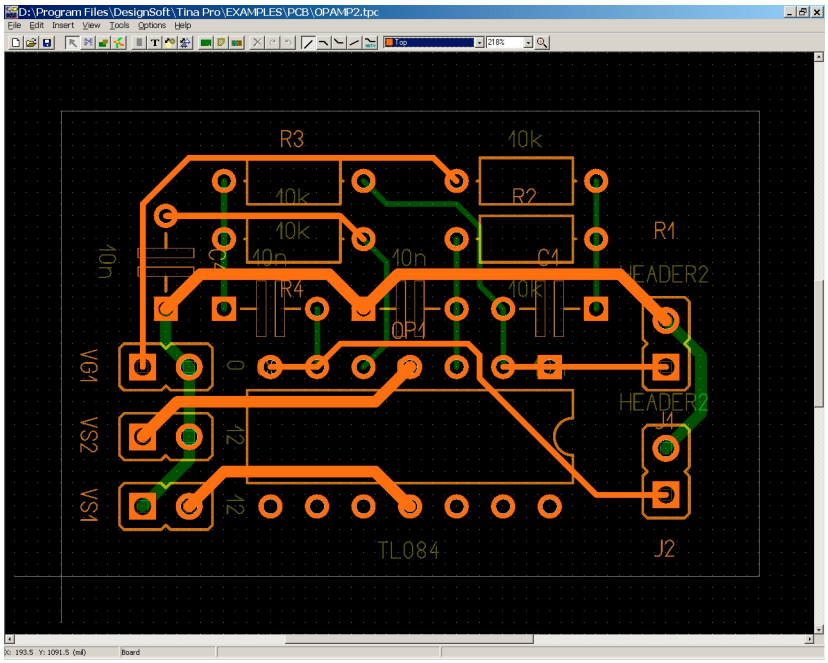
While all the parts and nets are placed, we need to adjust their positions for good placement and easier routing. Click and drag the parts to the position as shown on the figure below. (Find "opamp2 placed.tpc" to check your results.)



Press F4 to reach the Net Editor and set net routing width. First, click on "Modify all" and enter 12.5 into "Track width" field. Then select power nets (Ground, VCC, -VCC) and set their width to 25mil.

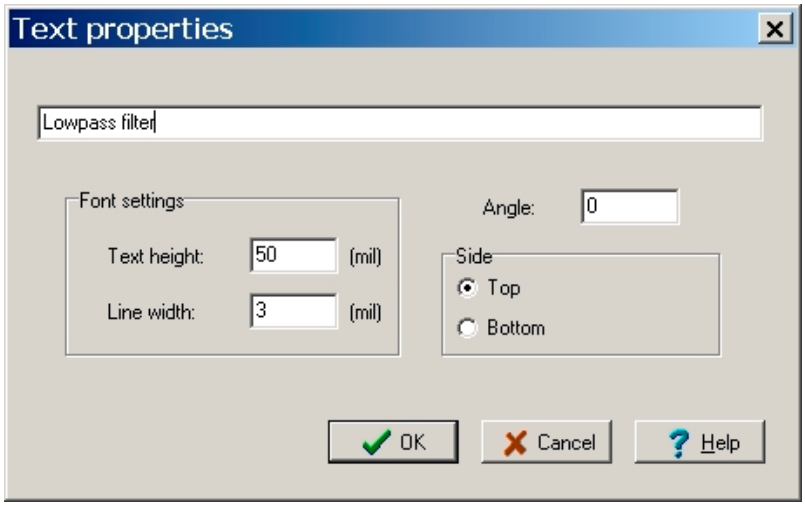


To automatically route the PCB, press the F5 button or select "Autoroute board" command from the Tools menu. The following screen will appear:

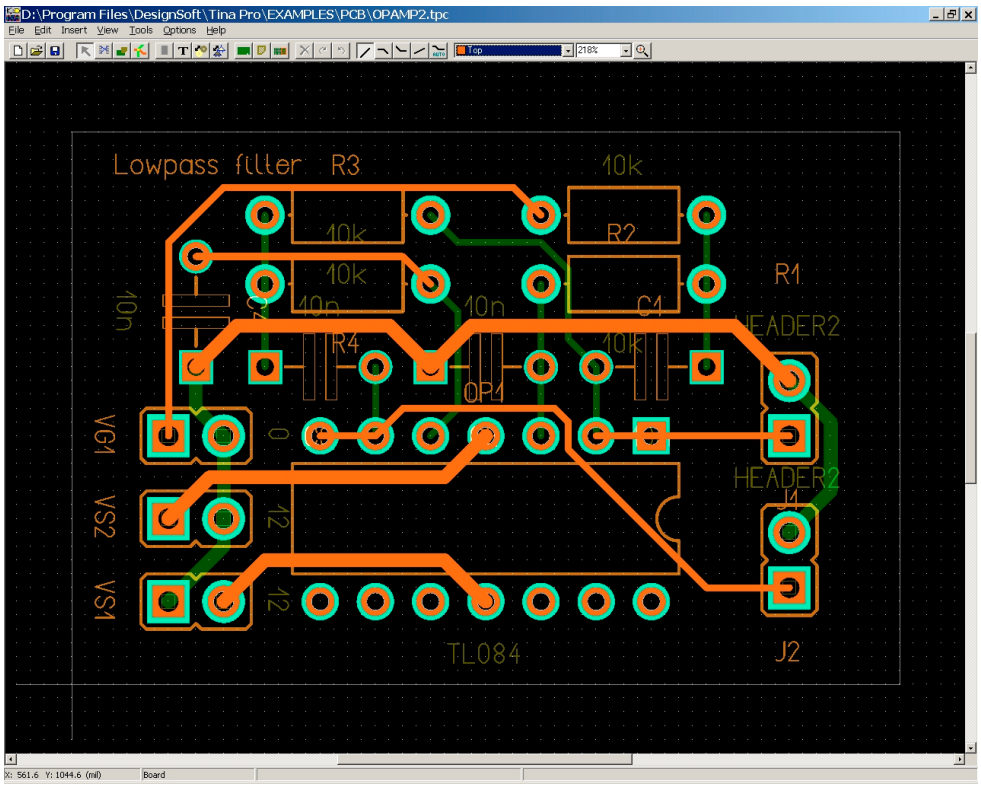


To see of everything is route correctly press F7 or select DRC (Design Rule Check from the Tools menu. The following message will appear:

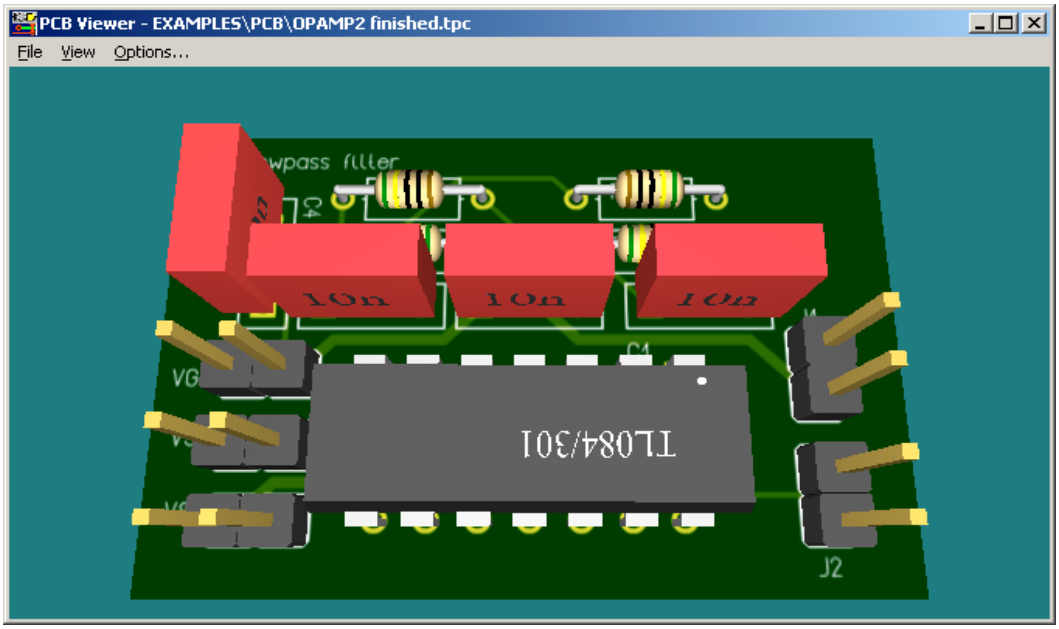
To finish our first simple design, let's add text to the silkscreen/assembly layer. Click the T button on the toolbar and make the settings in the dialog that appears:



Enter the text into the empty upper field and press the OK button. The text will be attached to the cursor. Move it to the location shown on the picture below and press the left mouse button to place the text.



Finally, you can check your design in full 3D. Press F3 or select 3D View from the View menu. After some calculation, the following window will appear.



You can rotate the 3D model to any direction by clicking with the mouse at any point. Hold down the left button and move the mouse to shift the viewpoint. You can also move the "camera" forward or backward to set a large view showing the complete PCB or to zoom in for more details. Use the right mouse button for this operation.

At this point, you will probably want to either print your design or create Gerber files for a manufacturer. To print use Print… from File menu.

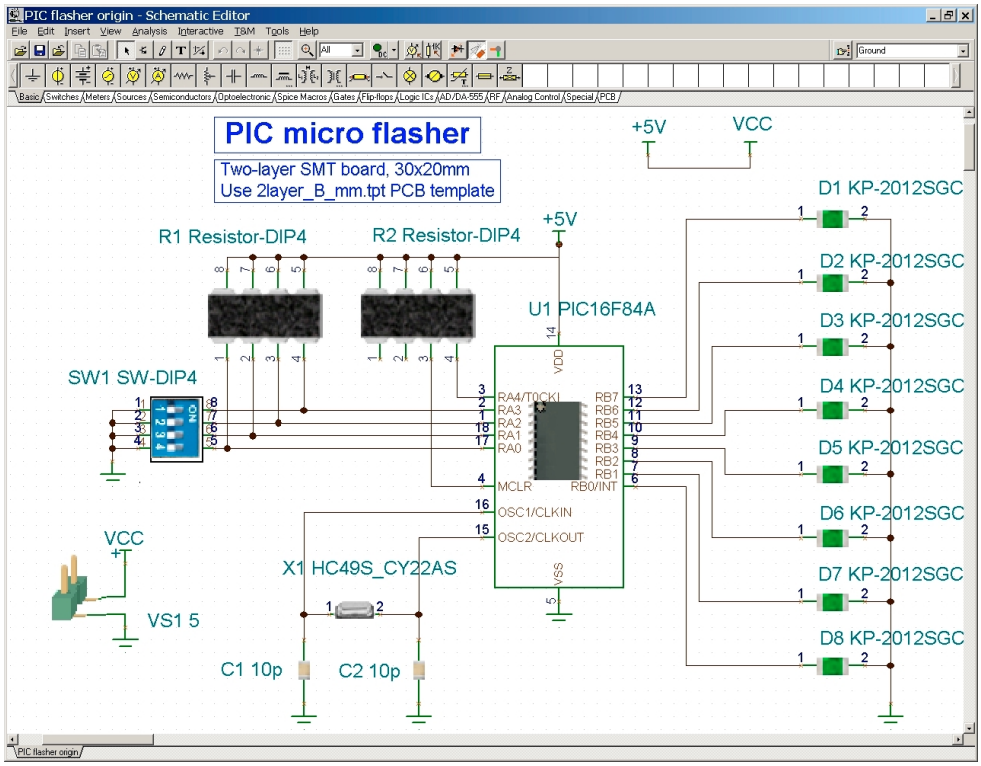
To obtain Gerber (RS-274X format) files to direct a photoplotter, choose Export Gerber file from the File menu. (Various Gerber options can be changed using the dialog for Gerber output settings under the Options menu.)

1.3 Advanced editing functions of TINA PCB's Layout editor

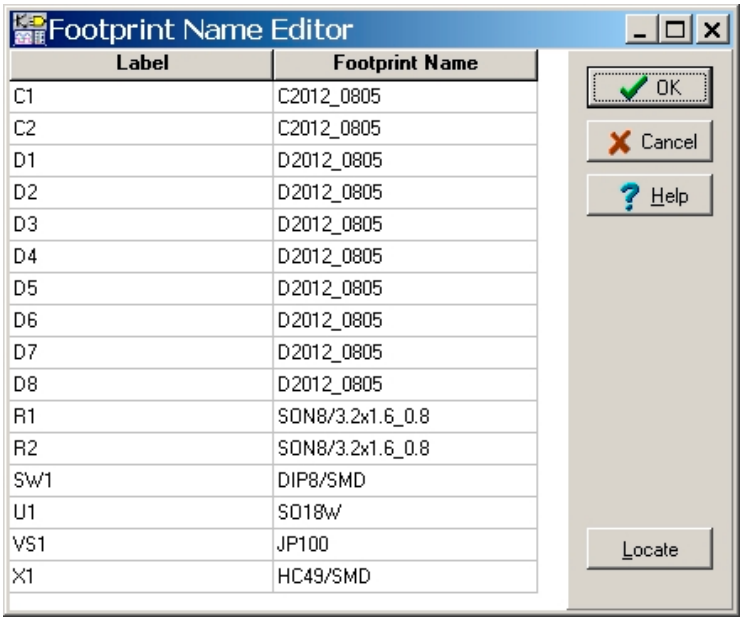
In practice, you may need to do some editing using TINA PCB's advanced editing features. This is described through examples in the next section.

CREATING A TWO-LAYER, DOUBLE-SIDED, SURFACE-MOUNT TECHNOLOGY BOARD

To get into TINA in more detail, open the second example, the file *PIC flasher origin.TSC* project from TINA's Examples/PCB folder. Press the 2D/3D View button in the toolbar and look at the schematic of the flasher.

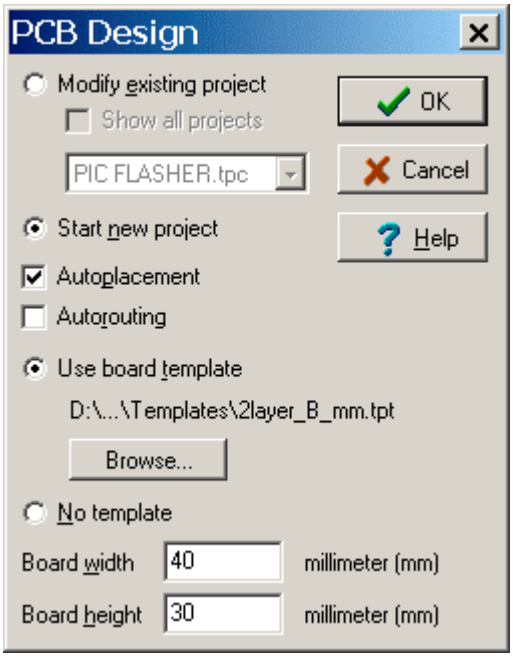


The schematic is PCB-ready–as you can verify by pressing the 2D/3D button, every part has a surface mount device (SMD) physical representation. Now, before we start the PCB wizard,click Tools/Footprint Name Editor… to check the footprints list.

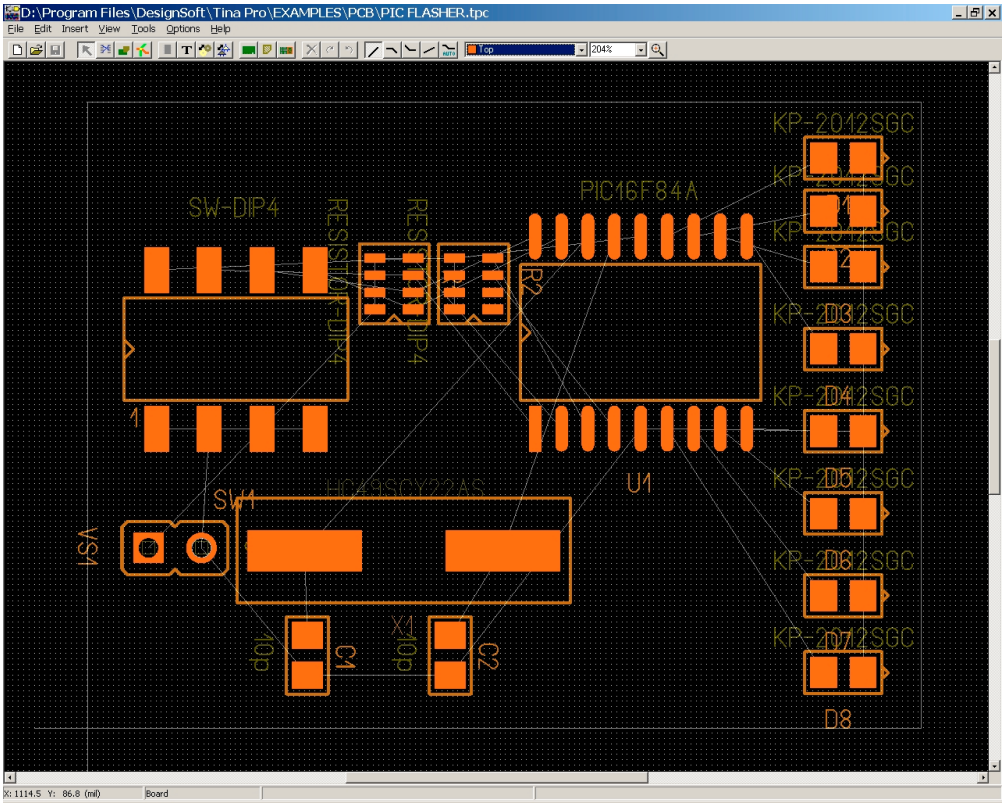


Since all the components appear to have a valid footprint name, we can start using the Tools/PCB Wizard. Set the "Start new project," check "Autoplacement" and "Use board template." Browse for the template file "2layer_B_mm.tpt."

Review actual physical parts, if possible. Be sure to allow for the area of all the components, mounting holes, and keep-away zones and make your best estimate of the values for Board width and Board height. Moreover, it is important to provide enough space between the components to allow for the placement of vias and tracks during routing. Enter 40mm length and 30mm width.



Press the OK button, ignore the Electric Rule Check warning, and save the board as PIC flasher.tpc.

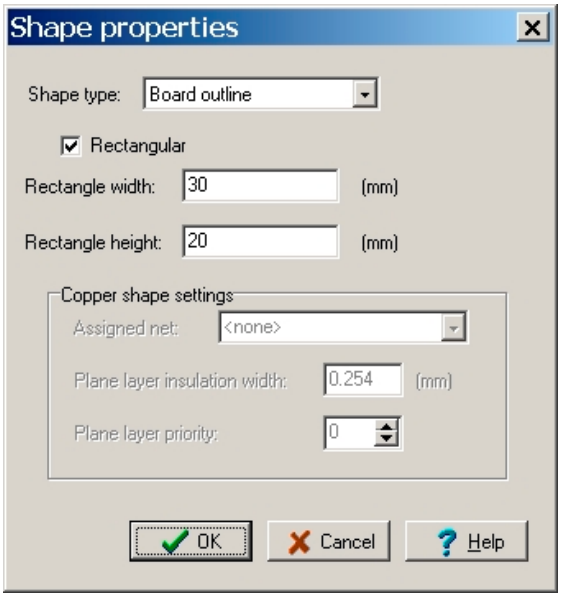


The components are placed in the close proximity to minimize the connection lengths, in a topology similar to that of the schematic, while still respecting the design rule settings. However convenient the result may be for autorouting, the designer usually has to make adjustments to the component layout to satisfy electrical, mechanical and other characteristics. Some of the considerations are—

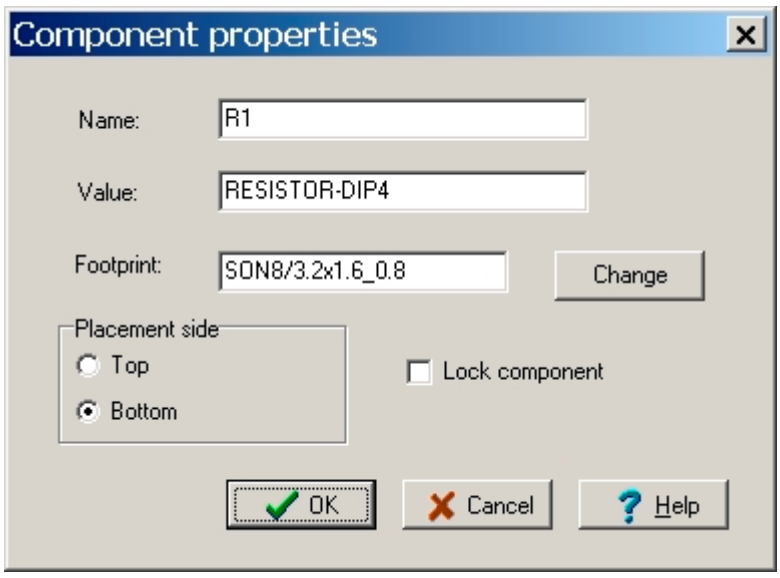
- the ohmic effect of a long and/or thin power tracethe length of a track from the signal source to the load in high-speed digital systems introduces reflections
- in analog situations, poor placement can lead to increased noise coupling
- allowance for automated parts placement clearance
- future serviceability of the PCB
- aesthetic values

These considerations influence the components' position and could be critical–not only in complex designs–but even in the simplest ones. For these reasons, one must still adjust parts placement manually.
Our circuit, although it is small and not very dense, has a few special requirements, namely to put the crystal closer to the microcontroller, to position the power supply connector, and to adjust the LEDs along the board.

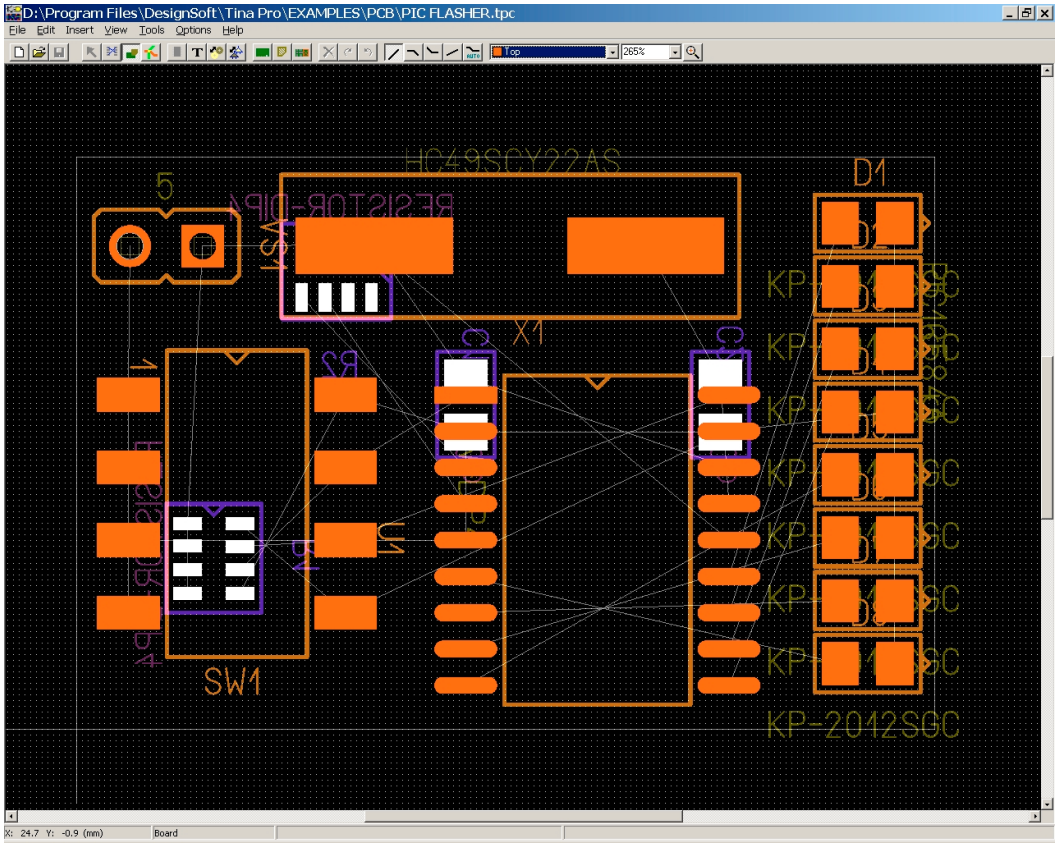
If you want to change the board size, click the "Draw/modify shapes" button . Let's try making the board smaller. You can double click on the middle of the board and enter the following values into the fields:



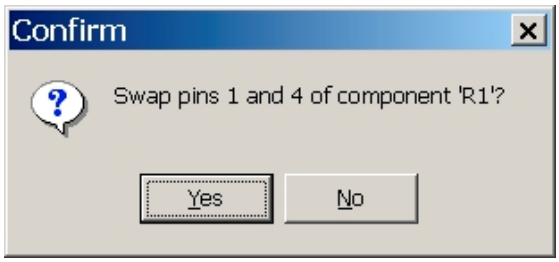
When you press OK, the board outline will shrink.
Now, before we begin routing, let's set the position of the components; place the power connector and the DIP switch on the left hand side and the LED bar on the right hand side. Place the capacitors and resistor networks on the bottom side by double clicking on the components and choosing Bottom Placement side on the dialog.



Compare your result to the file \Examples\PCB\PIC flasher placed.tpc.

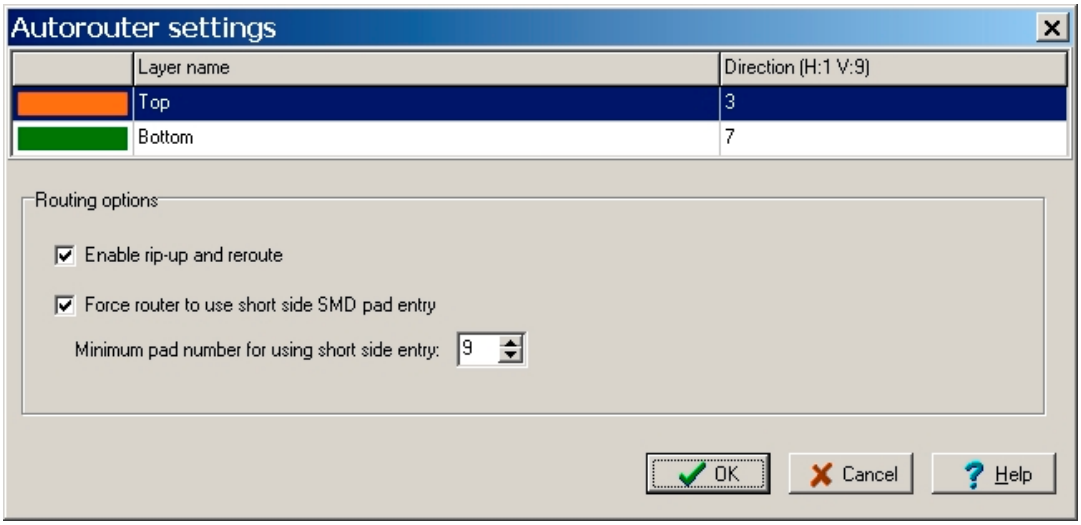


In order to decrease route length, swap R1 pins connected to SW1. Pin swapping is allowable if identically functioning pins are to be exchanged, such as pins of resistors, capacitors, etc. Click on the Pinswap button on the toolbar to pick up the tool, click on pad 1 of R1 (the upper right), and–finally–pad 4 of R1. The following window should come up:



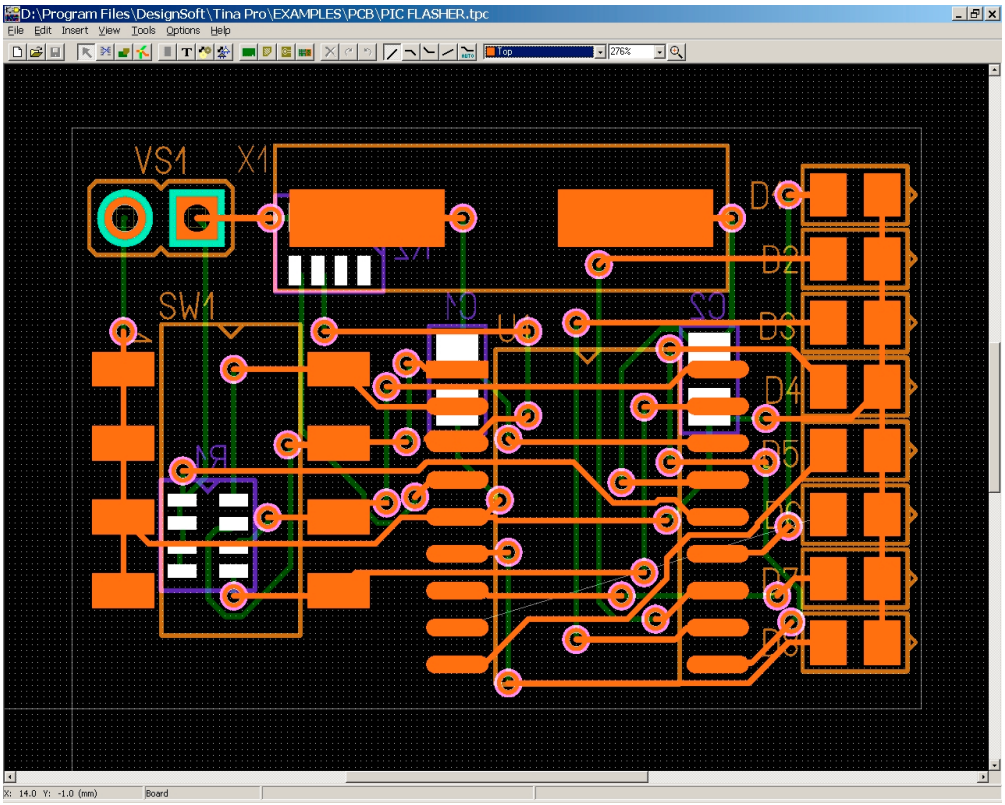
Press the Yes button, then do the same with R1 pad 2,3 and R2 pad 3,4.
Note that a pin swap changes the original connections, so we must update the original schematic later to maintain the correspondence between the schematic and the board taking into account the changes we made to the board while using PCB Designer. This process, called backannotation, has to be completed whenever a pin/gate swap and/or component renaming have been performed.

Signal planes (in our present example, the top and bottom layers) generally are given preferred trace directions up and down in one layer and left and right in the other layer. To set these trace directions, click on Options/Autorouter settings. The Autorouter settings are set to our preferred direction by choosing an integer number from 1 to 9. A value of 1 forces the router to heavily emphasize horizontal lines, while a value of 9 forces it to use vertical lines. 5 tells the router not to care about horizontal or vertical preference. Choosing the extreme values (1 and 9 for a pair) is usually too strict, so we choose to enter 3 for the top layer and 7 for the bottom.

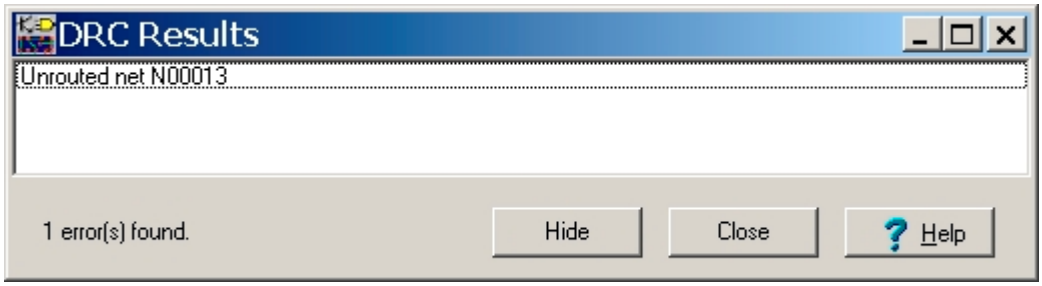


Also on this panel, check "Force router to use short side SMD pad entry" with pad number 9 constraining the router to connect SMD pads on their short side if the component has at least 9 pins. This option can be very used to preserve the gaps between SMD pads for track routing. Because of these choices, R1, R2 and SW1 are allowed to route freely, as half of the pins are connected together, while U1 pads connect on the short side.

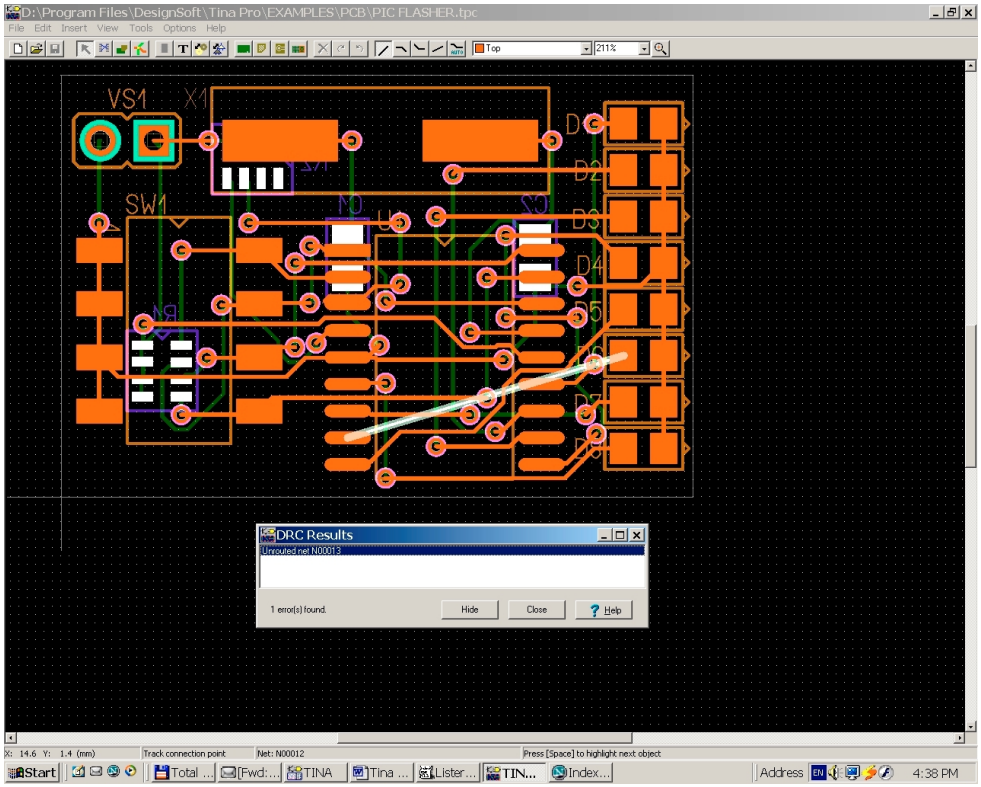
After these moves, press Ctrl+F5 to route the PCB automatically. You can follow the autorouter as it makes the electrical connections among the components of the entire boards. First the power and ground nets are connected, then signals are routed. If necessary, the program will rip-up tracks and reroute the unconnected nets. The following result will appear:



You can seee that there is a net left unconnected. (Note: this shortcoming will be removed in later (relative to February 2006) versions of PCB Designer. If you are using a later version, there may very well not be any unconnected traces). Fortunately, the DLC utility will examinine your design and reveal any unconnected traces. Run DRC by pressing F7: the DRC Results window will appear, highlighting the corresponding nets.



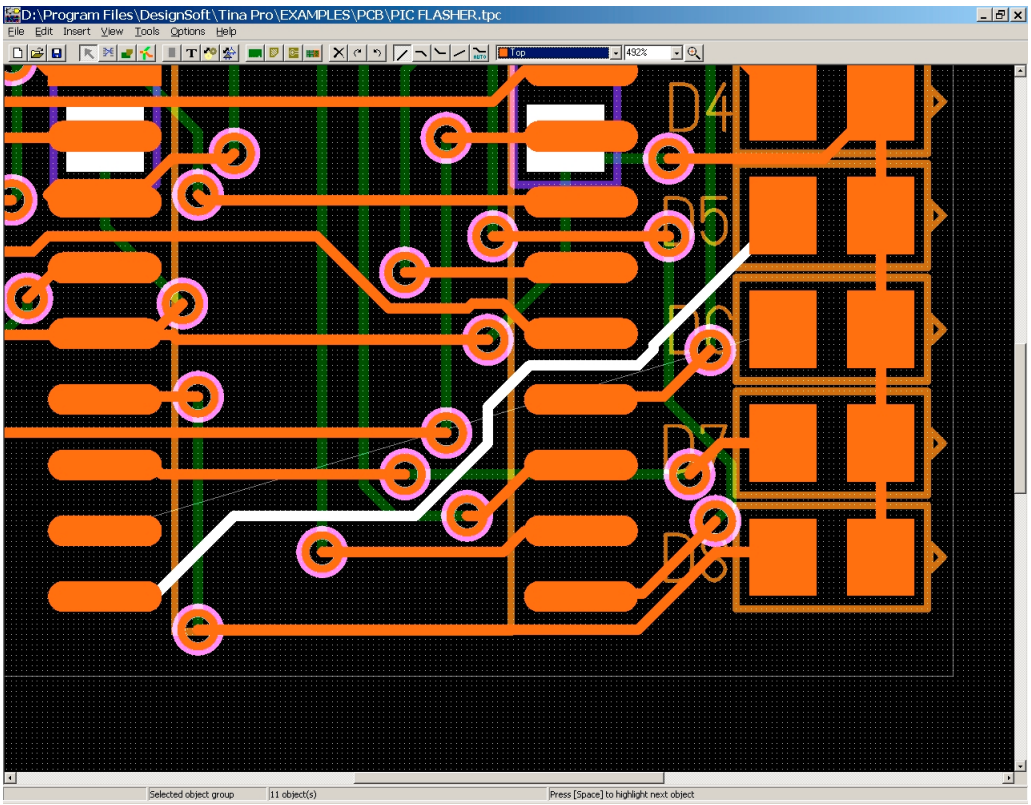
You should browse and correct any errors DRC reports. If you double click on the text 'Unrouted net N00013,' the program magnifies and highlights the selected net while centering the position of the selected objects.



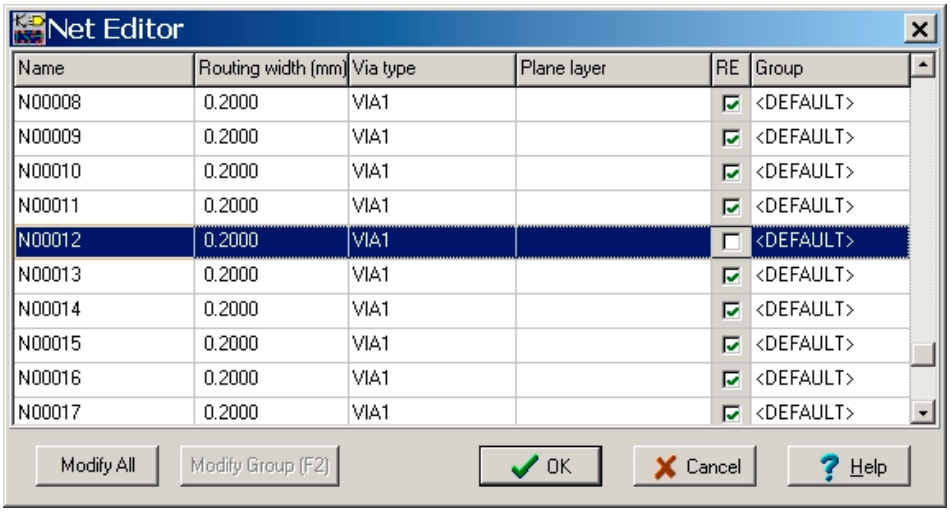
In order to fully route the board, we can use the manual route modes to make space for the unconnected tracks or delete crossing tracks and reroute them in a different order. Working in manual route, you can direct routing wherever necessary. You can move existing segments of tracks, remove segments, or create new segments.

Proceeding step by step, we will use autorouting to route the last trace.

First, press the , the select button on the toolbar, then hold down the Shift key and click the track that connects U1 pad 9 to D5 (see picture below), then press the Delete key to remove the track. This makes room for the unconneted net.

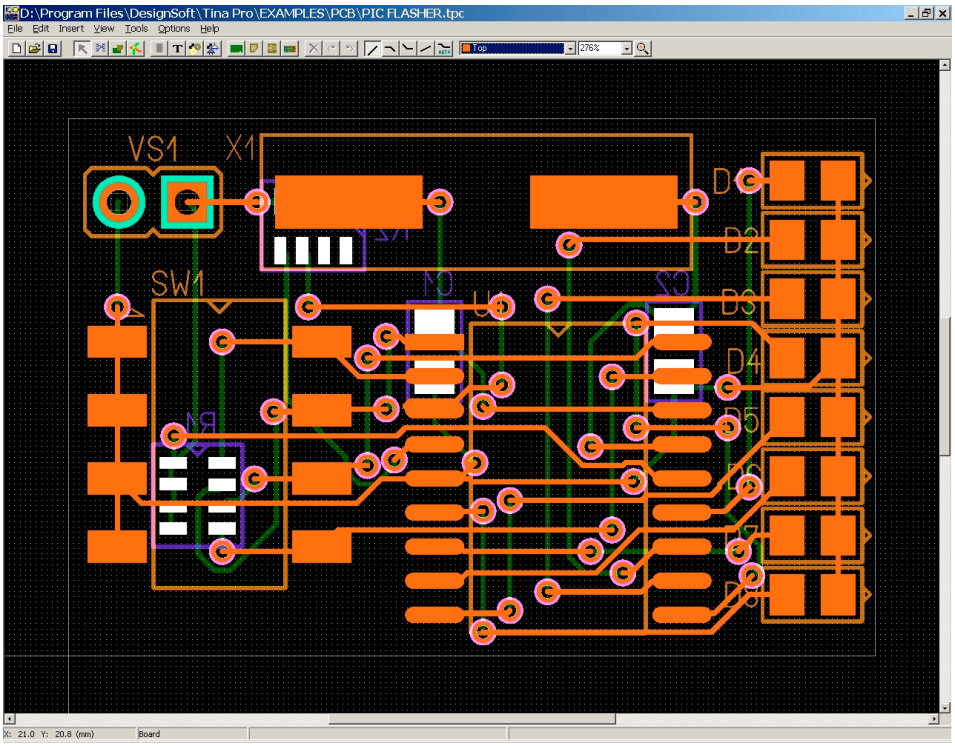


Now press F4 to invoke the net editor. Disable N00012, the previously removed connection. This will prevent the autorouter from reconnecting the net. Leave N00013 routing enabled.



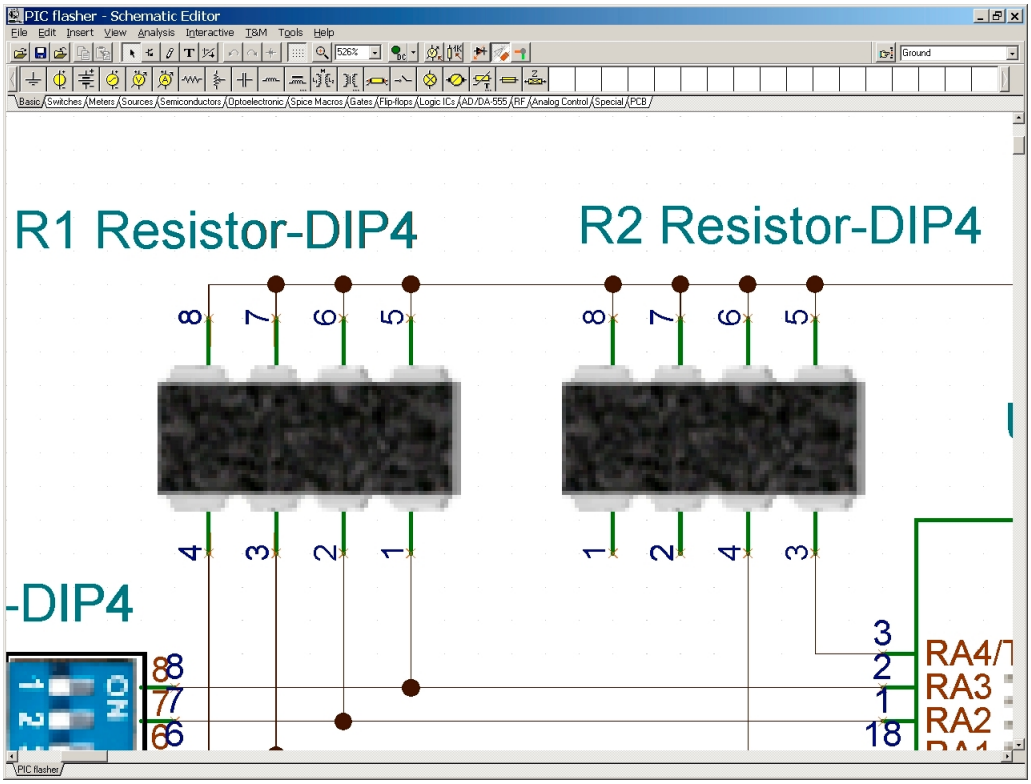
Click OK and press F5 and the autorouter will connect all the enabled nets. Next, enable N00012 by pressing F4, checking RE, clicking OK and pressing F5 to autoroute the last net.

Let's see if our manual intervention has worked. Press F7 to perform DRC to verify that there are no errors.

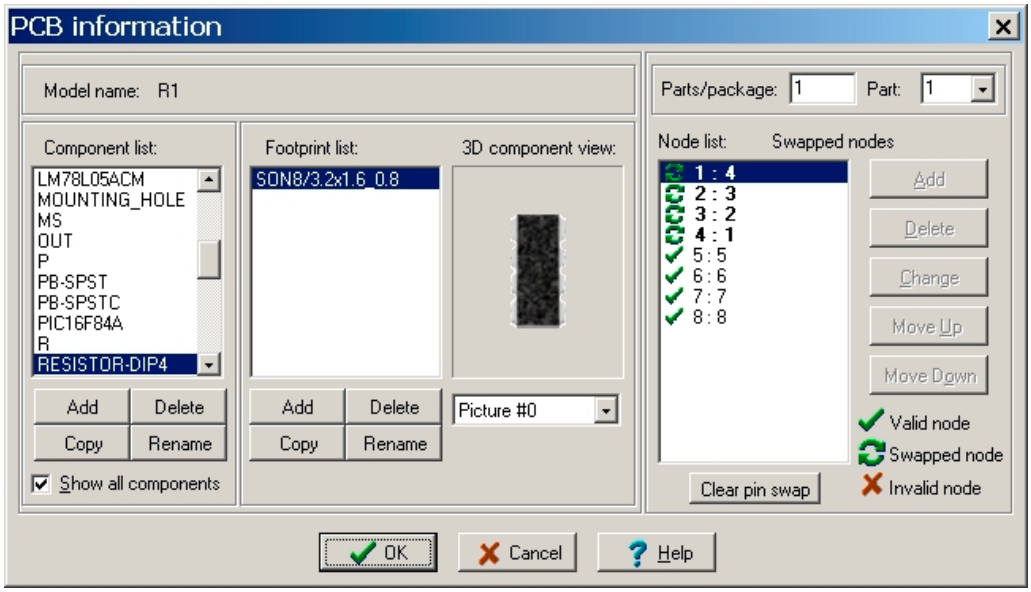


Now, let's synchronize the PCB and schematic files. First, choose Export Tina backannotation file from the File menu to save the changes into PIC flasher origin.ban. Start TINA Pro and click on Backannotate… under the Tools menu and select the same file you have just saved. Click OK and TINA will read and update the original schematic.

Take a close look at the resistor networks–the pin order reflects the result of the pinswap.

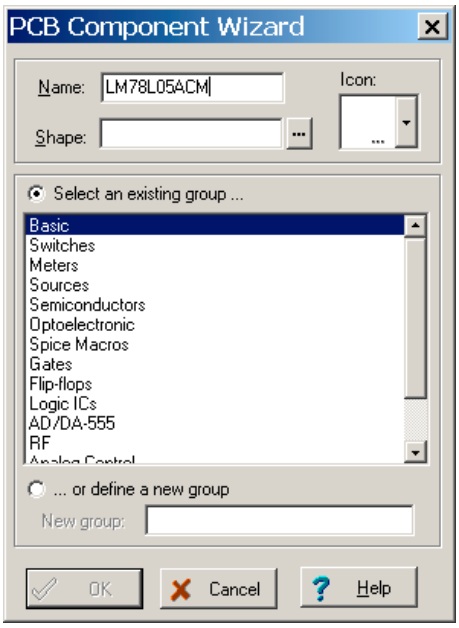


You can get to the PCB Information dialog by doubling clicking on R1 and pressing ... in the Footprint Name field. In the right hand window, TINA presents the swapped nodes in larger, bold type. Save this file as PIC flasher.TSC.

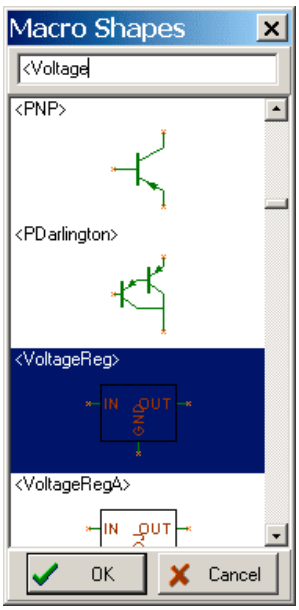


CREATING PCB COMPONENTS

Now, let's see how to create our own PCB components for use in a PCB design. We place an LM78L05ACM (plastic SO-8 package) voltage regulator on the schematic to make the circuit +12V powerable. If we do not want to simulate the circuit, TINA gives specific tool to create PCB symbol. So, click PCB Component Wizard… in the Tools menu and enter the name of the component in the Name field.

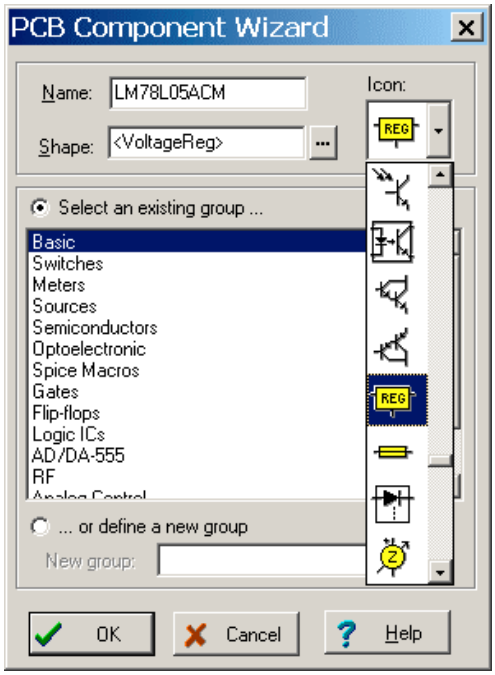


Click the button to choose the component Shape from the library. Enter a few letters from macro shape name: <VoltageReg>, then click OK.

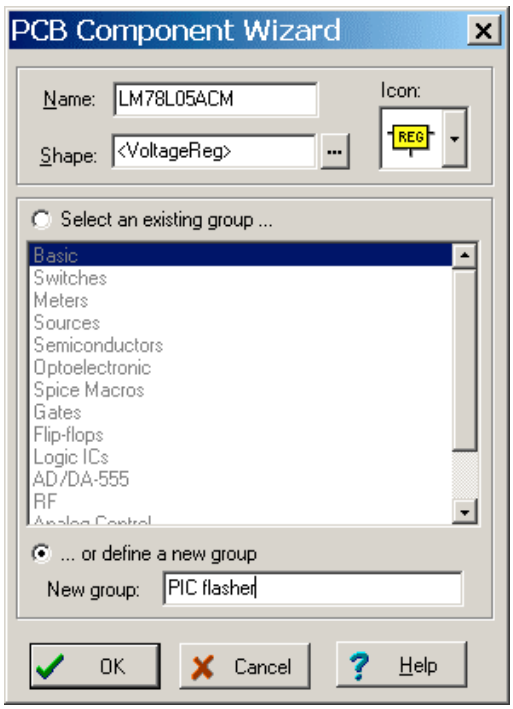


If you do not find an appropriate macro shape for the new component, use the Design Suite's Schematic Symbol Editor.

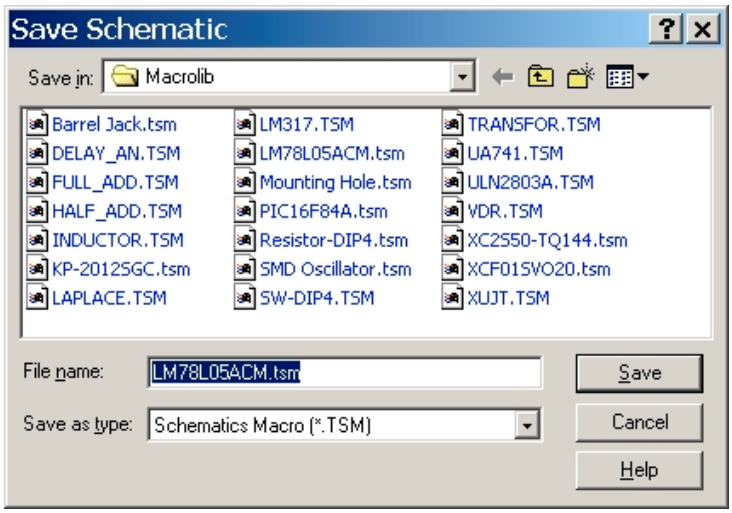
Choose the REG icon from the Icon drop down list.



So that we will be able to access a new PCB component in TINA, we should add it to one of thecomponent groups. This time, you can define a new group for our component, called PIC flasher, then press the OK button.

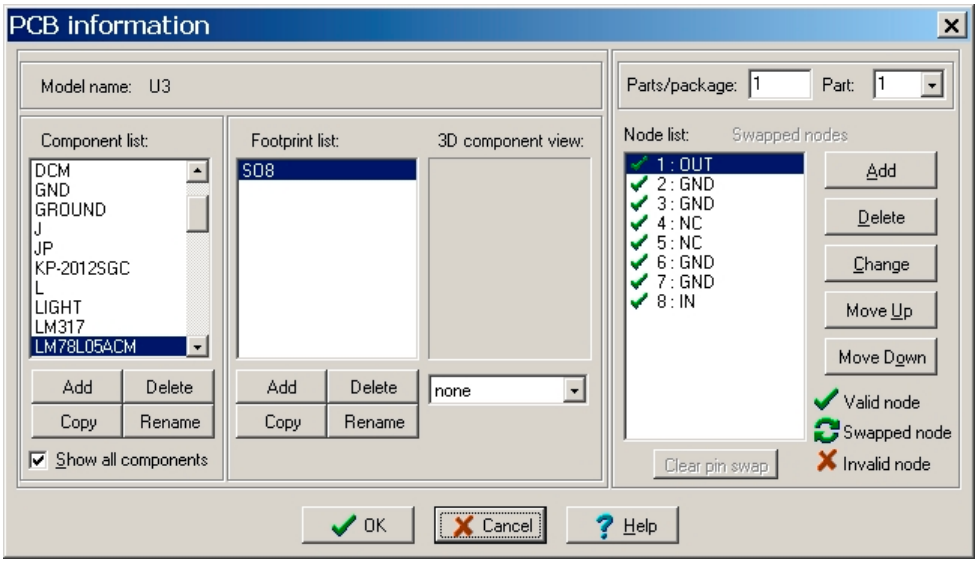


Finally, you may save the new PCB component macro into the Macrolib folder.

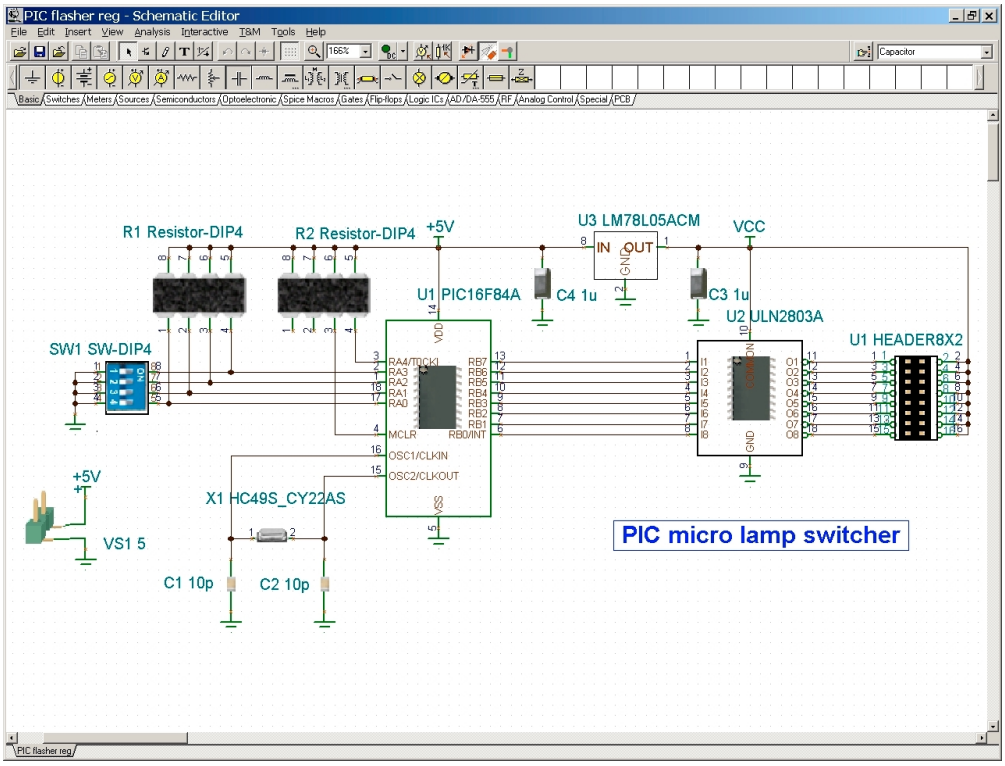


Replace the short circuit (on the schematic) between Vcc and +5V with the new component and double-click on the schematic symbol of the regulator. Enter the PCB information:

1. Click in the Footprint Name edit line on the button.
2. Click the Add button on the Component list area and type LM78L05ACM. Then press OK.
3. Click the Add button on the Footprint list area and choose SO8 from the SMDIC category.
4. Build the part node list with the help of the component data sheet (http://www.national.com/ds.cgi/LM/LM78L05.pdf) : click Add, then select OUT from the Change Node List and press OK. Repeat these steps until all of the pins are defined and, at last, click OK.



By this point, we have set every parameter and have a "PCB-ready" component. To verify the part correctness, you can open PIC flasher reg.TSC and check it with ERC.



As the electric type of U3 pin 1 (OUT) is defined to be an output and is connected to the power pins of U1 and U2, you will encounter ERC errors when you call PCB Wizard or perform an ERC. But knowing that U2 is the power source for the ICs, we can safely disregard this error.

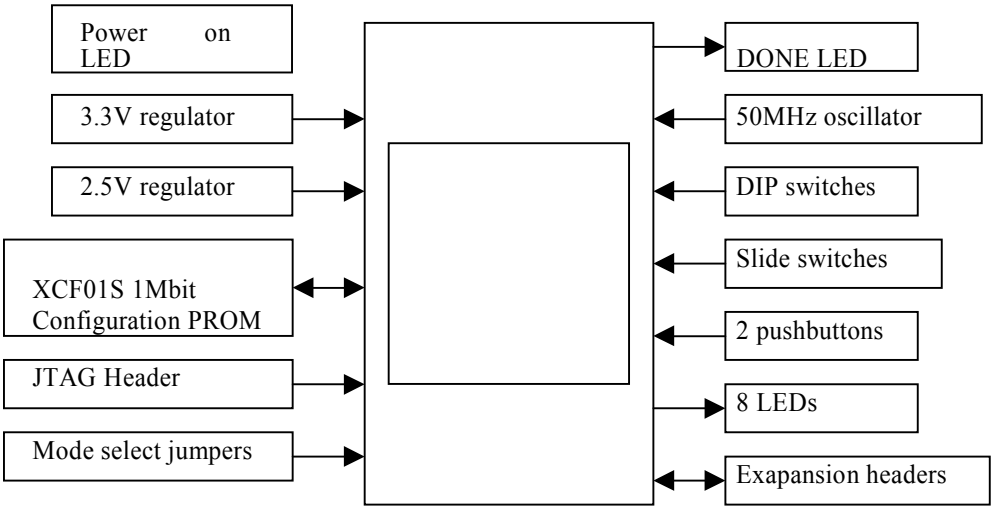
CREATING 4 LAYER PCB LAYOUT

This chapter provides an introduction to 4 layer PCB design. We will follow the entire process and design a medium size circuit PCB. This will demonstrate the major concepts and introduce the settings, techniques, and tools required. We will emphasize the concepts where they differ from the previous single and double layer designs. Many phases of the example can be found in the \Examples\PCB directory, such as:

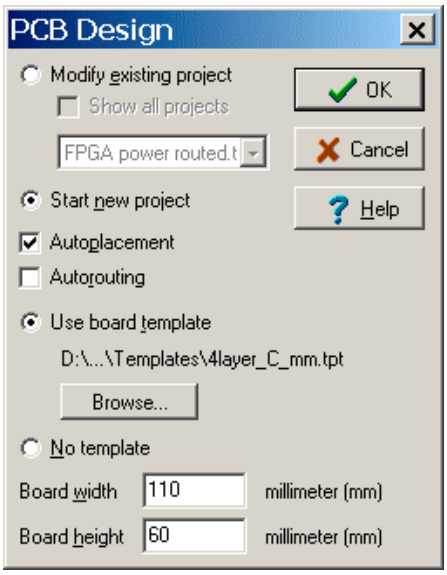
Schematic files	
FPGA origin.tsc	original schematic file
FPGA.tsc	schematic file (backannotated, after renumbering)

PCB files	
FPGA placed.tpc	design parameters set, components placed
FPGA placed split.tpc	as above with power plane splitting
FPGA Spartan power routed.tpc	net properties set and Spartan FPGA chip power routed
FPGA Spartan power routed split.tpc	as above with power plane splitting
FPGA all power routed.tpc	power routed
FPGA all power routed split.tpc	as above with power plane splitting
FPGA routed.tpc	all connections routed
FPGA finished.tpc	optionally pin/gate swapped and renumbered, routed, silkscreen adjusted, documentation layers finalized pcb file

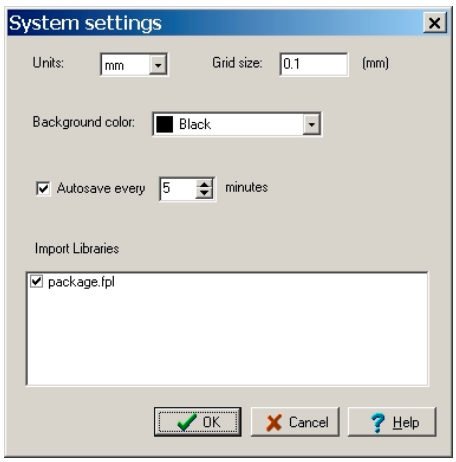
The block diagram of the circuit we will design is shown in the figure below. The main
component is a field programmable gate array (FPGA) from Xilinx, Inc. In this circuit,
we will use the FPGA with a few pushbutton switches as inputs and LEDs as outputs.
Many of the FPGA IO pins can be used freely for general purposes and are brought out on the connector J1.
The board contains a power connector for an external 5-volt supply, a programming interface for the FPGA, and some miscellaneous resistors and capacitors.



For the complete circuit digram, open FPGA origin.TSC (the backannoteted version saved as FPGA.tsc.) All the footprints are named, the schematic is ready-to-use for layout design. Just click on the PCB Wizard… set "Start new project", check "Autoplacement", and use board template 4layer_C_mm.tpt (work in metric units because the components' physical dimensions are defined in the metric system). For the best routing performance, taking the smallest pitch size (0.5mm) as reference, we set the Grid size parameter to 0.1mm which will control the visible grid, the parts placement, and routing grids.
Enter the width (110mm) and height (60mm), then click OK.



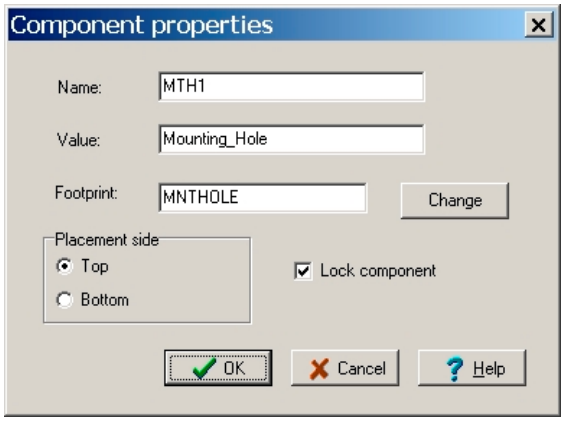
After exporting the netlist from TINA, you should check a few parameters in the PCB editor. First, select Option/System setting. Make sure that PACKAGE.FPL is checked.



4.1 Placing parts

To make the screen less cluttered, let us turn off a few layers at this point. Select Option/Layer Settings, press Uncheck All, and check Assembly Drawing Top and Bottom layers.
You are now ready to place parts on your design. To get into parts placement mode, make sure that the Select/Move components/tracks tool is selected. A good starting task is to place the non-electrical components on our board, the mounting holes in each corner.

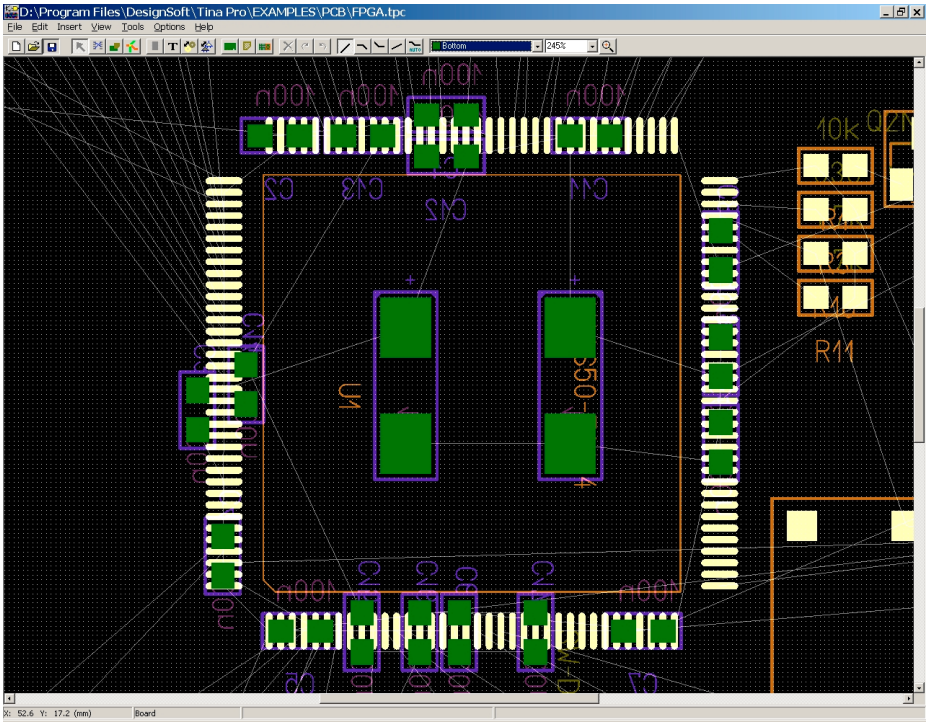
Every non-electrical component (mounting hole, rubber foot, enclosure…) symbol has to be placed on the TINA schematic before making a netlist. In the case when no footprint should be placed on the board (e.g. rubber foot) then the componet has NOPCB footprint name in TINA schematic.
Now, place the mounting holes at the corner.
Since we don't want to accidentally move the part, right click, select Component Properties and check the box labeled Lock component.



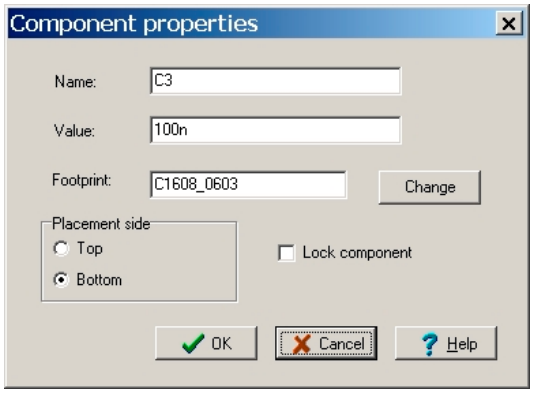
Now you can place the rest of your components. You will probably want to print out your schematics so that you can see where the components are supposed to go in relation to each other. When you pick up a component, the airwire for that component will appear to show you the connections to other parts.

When placing components, you may want to work on a coarser grid. Right now, the grid is set at 0.1 mm. You can change this by selecting Options/System Settings and then changing the Grid setting.

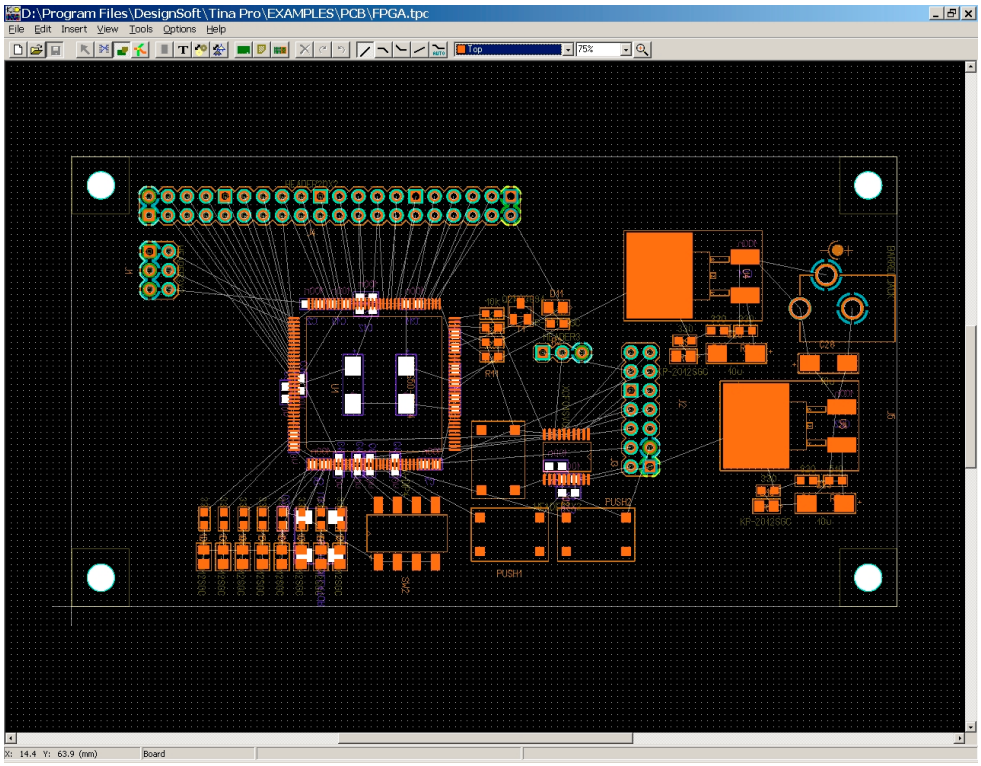
Start placing the components on your board. Begin by placing the power connector and voltage regulators on the right side of the board. Allow enough room for the power dissipating copper area. Place the FPGA in the left center with the 40 pin connector above, and LED and switches on the bottom. Try to keep components that belong together near each other.
Put the buffer and filter capacitors of the FPGA and flash memory on the bottom side of the board as close as possible to power pins of the chip, the smaller ones right under the leads, the bigger ones around the middle of the package.



To place a part on the opposite layer, right click on it, choose Component properties and select bottom placement side.



When you are done, your board should look something like this.



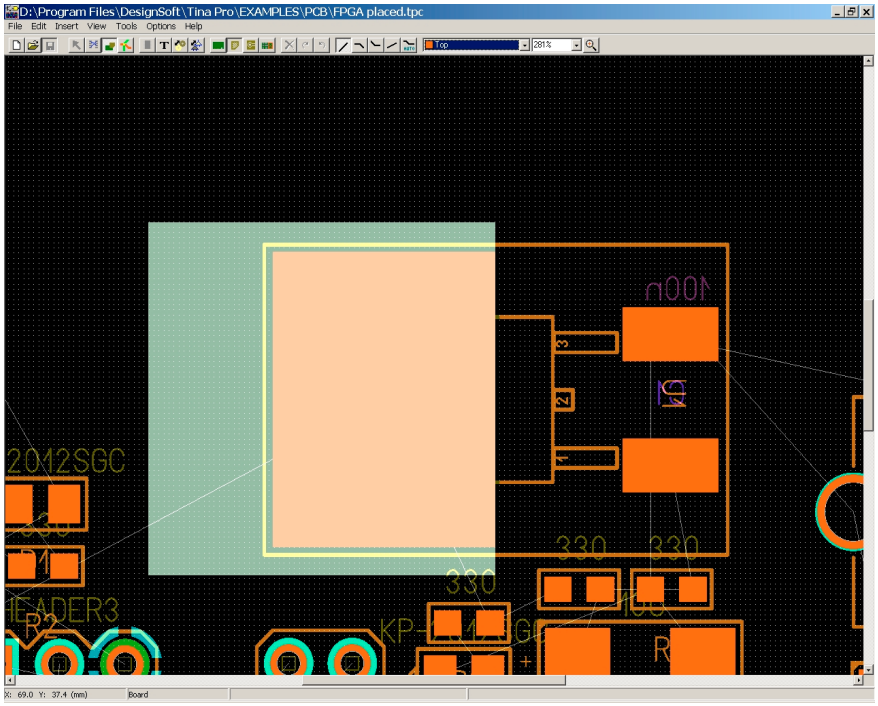
The silkscreen is a bit messy, but we will deal with that later. In fact, during routing the silkscreen can get in the way, so you may turn off the silkscreen and assembly layers now, just as you did earlier to suppress the two inner layers.

Now, you may save your design as FPGA placed.tpc.

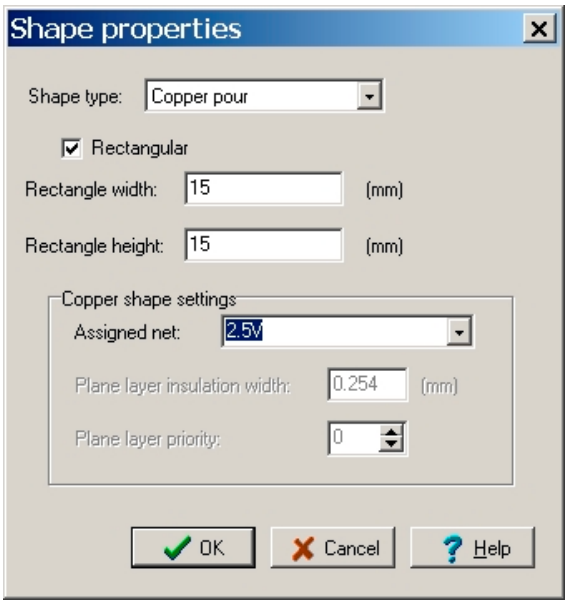
4.2 Draw copper areas for voltage regulators

(Go on with your own created file or open FPGA placed.tpc in the \EXAMPLES\PCB directory.)
Copper areas can be used for noise suppression, shielding, to draw heat away from components that tend to get hot, to isolate signals, or to provide small voltage planes. Now, to enhance the maximum power dissipation of the voltage regulator circuits (U4,5), we draw a 15 by 15mm area of copper on the top layer to widen the regulator heatsink surface.

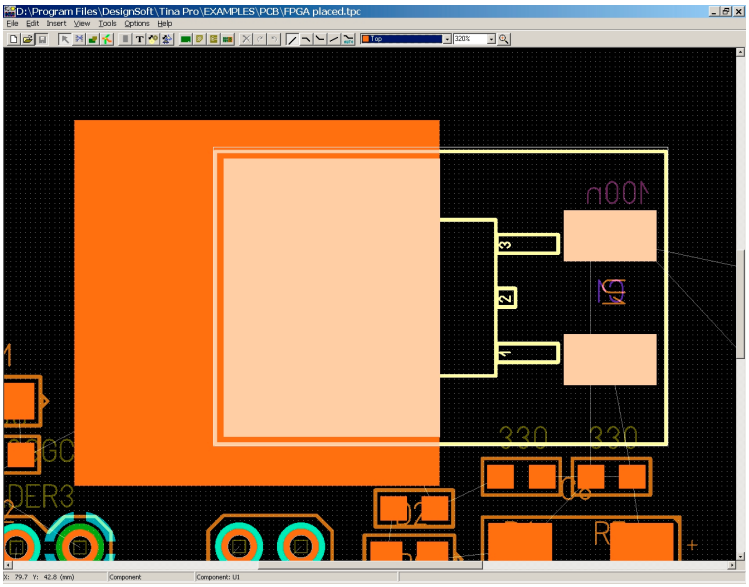
Choose "Add Cooper pour" icon from the toolbar then click on the upper left corner, drag the mouse towards the lower right hand corner, and finally click the left button.



When you double click on the area, you can enter the parameters exactly. Do not forget to check the shape type and select Assigned net 2.5V. Normally, copper pour creates voids where there are tracks or pads except for the Assigned net. (See Options/Design Parameters). The other shape type is the copper fill area which is solid.



Now click on the copper pour, hold down the left mouse button and position the rectangle, expanding leftward to overlap the heatsink.



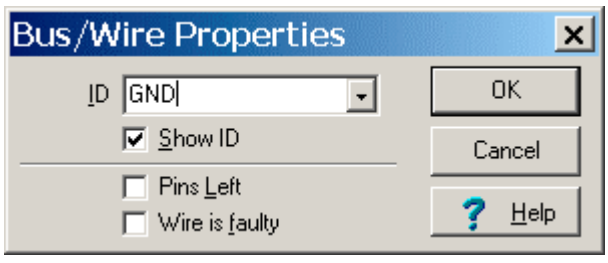
Finally, repeat these operations for the other voltage regulator and save your design. Note, you can find this state of the design if you open \Examples\PCB\FPGA placed.TSC.

4.3 Assigning and routing Ground and Power

In any design, it is usually wise to route all power and ground connections before doing anything else. On a thru-hole technology board, this is very easy because connections can be made to the solid plane as the pins pass through the board. On a SMT board, the power and ground pads need to be routed by vias to the appropriate plane using ”thermal reliefs”. Usually, the designer enables routing for the power and ground nets, while disabling routing of all the other signals. After routing power and ground nets, the designer will disable them and enable all the other signals to route the remaining signals.

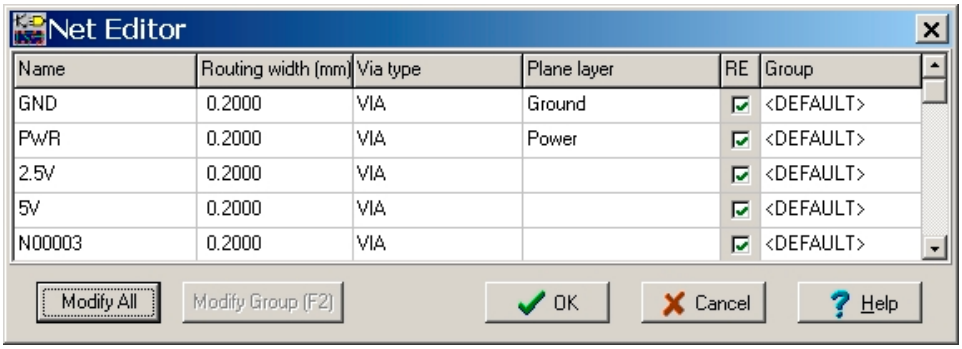
Before routing, we need to set up our design so that the PCB editor knows that the two planes are associated with particular nets. (Interior plane layers are typically used for power and ground.) The most convenient way to establish the mapping of planes to netlists is to assign a label to a wire of the net (as we did) while in the TINA schematic editor. We have already placed such labels in FPGA.TSC at the output of the power regulators. (See FPGA origin.TSC at X:485, Y:880; X:440, Y:930) The GND label will inform TINA PCB that the solid plane on layer 2 (Ground) is asssigned to the net, while the PWR label designates layer 3 (Power).

You can handle other nets in the same fashion, by double clicking on the wire and modifying the ID in TINA schematic.



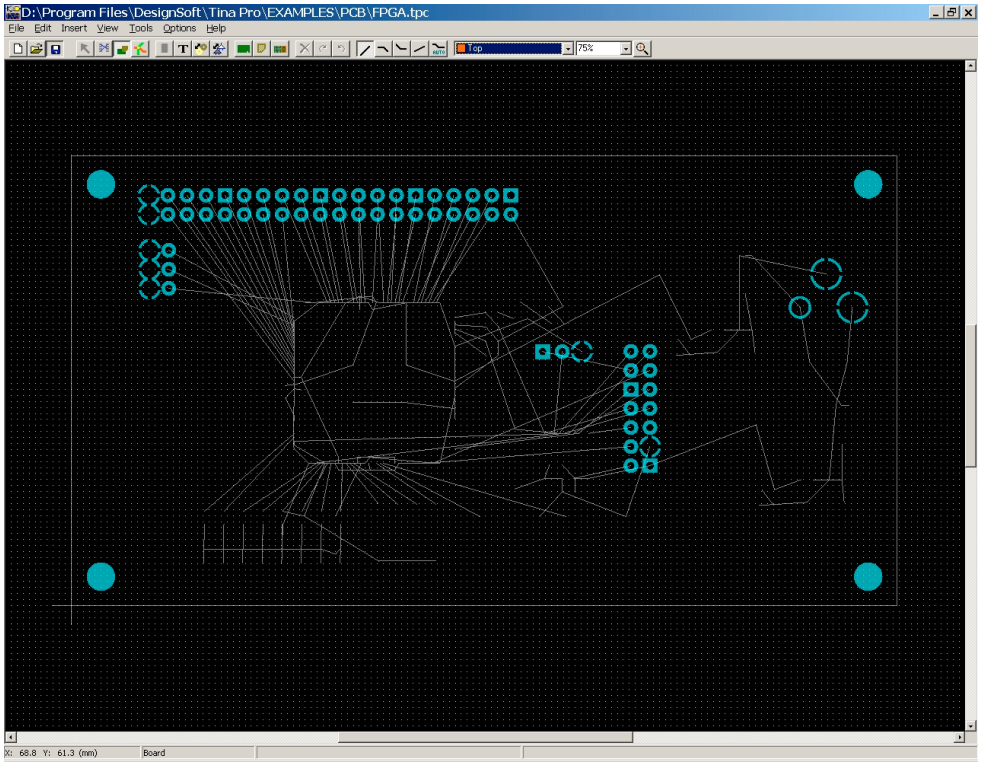
Note, only GND and PWR IDs have special effect on the plane layer allocation; other net names are just for clarity to help you recognize the source of the nets in the PCB editor, eg. 2.5V in this design. It is always advisable to name the significant nets for easier operation later when using the PCB editor.

Open the Net Editor and check the result.



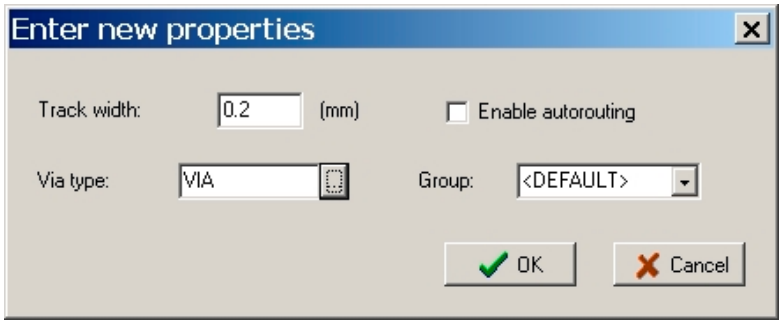
You can attach any nets to any plane layer in PCB editor also, but it is easier to do this in TINA schematic as described.

To view plane layers, click Cancel while in the Net Editor and choose Option/Layer settings, press Uncheck All and check Ground. The thru-holes are already connected by thermal reliefs.

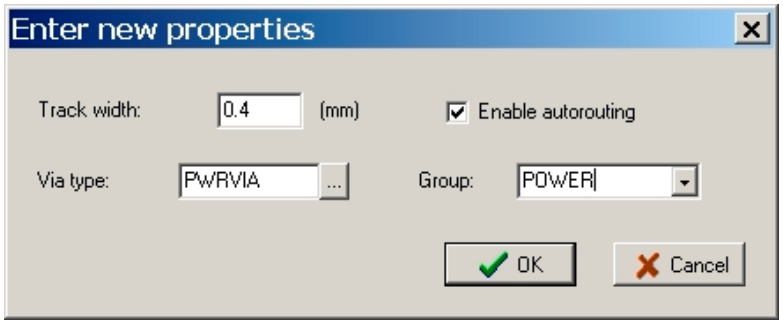


You can now see all of the connections to the ground plane. You can do the same thing for the power plane: Option/Layer settings, uncheck Ground and check Power.

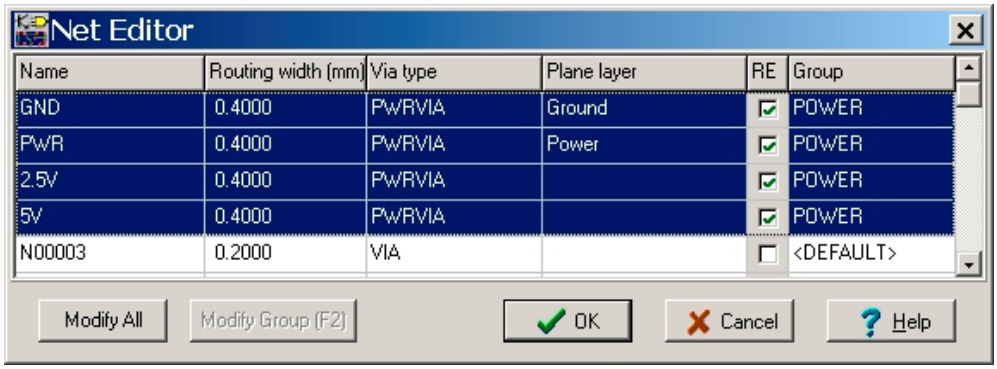
At this point, we have only routed the thru-holes for power and ground connections. On a surface mount technology board, we should fanout[1] the board with only the power/ground net enabled. In the Net Editor (F4) press "Modify All" button to uncheck "Enable autorouting".



Select the ground and power nets and create the net group POWER; simply type POWER in the Group field. Enter 0.4mm to Track width and check Enable autorouting with via type PWRVIA.



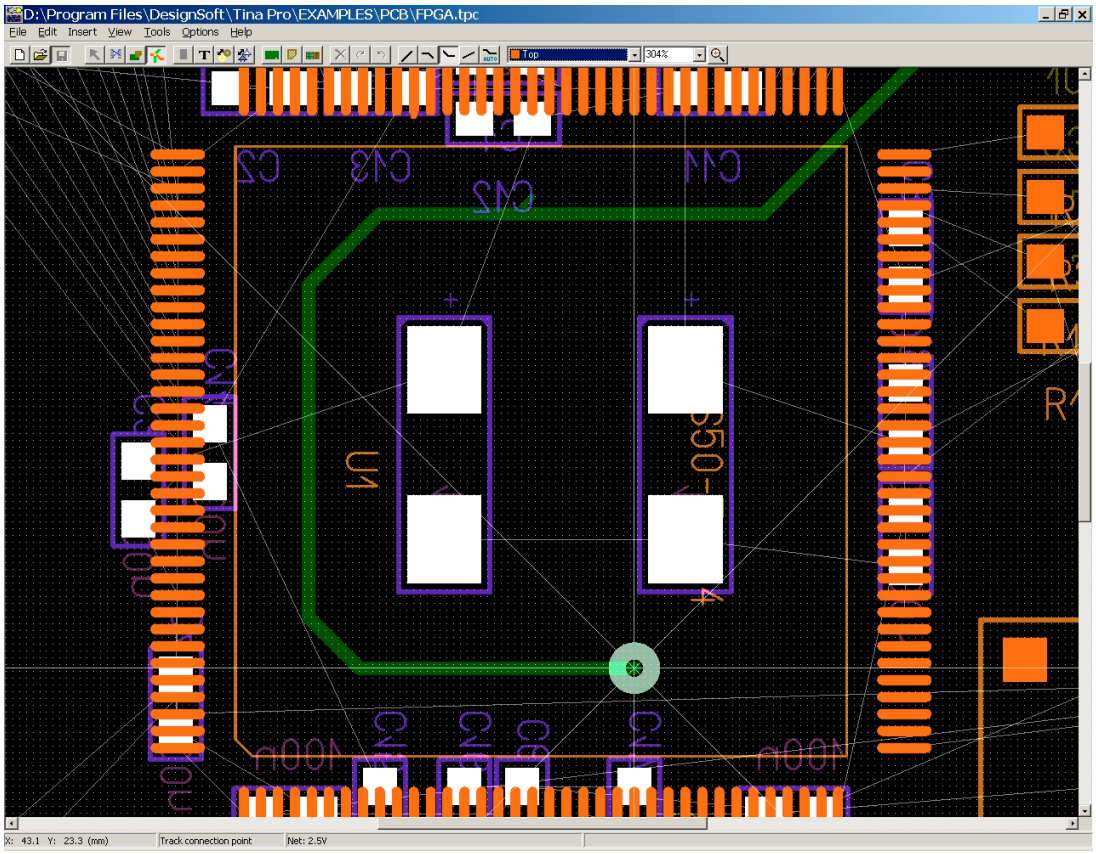
The Net Editor should look like this.



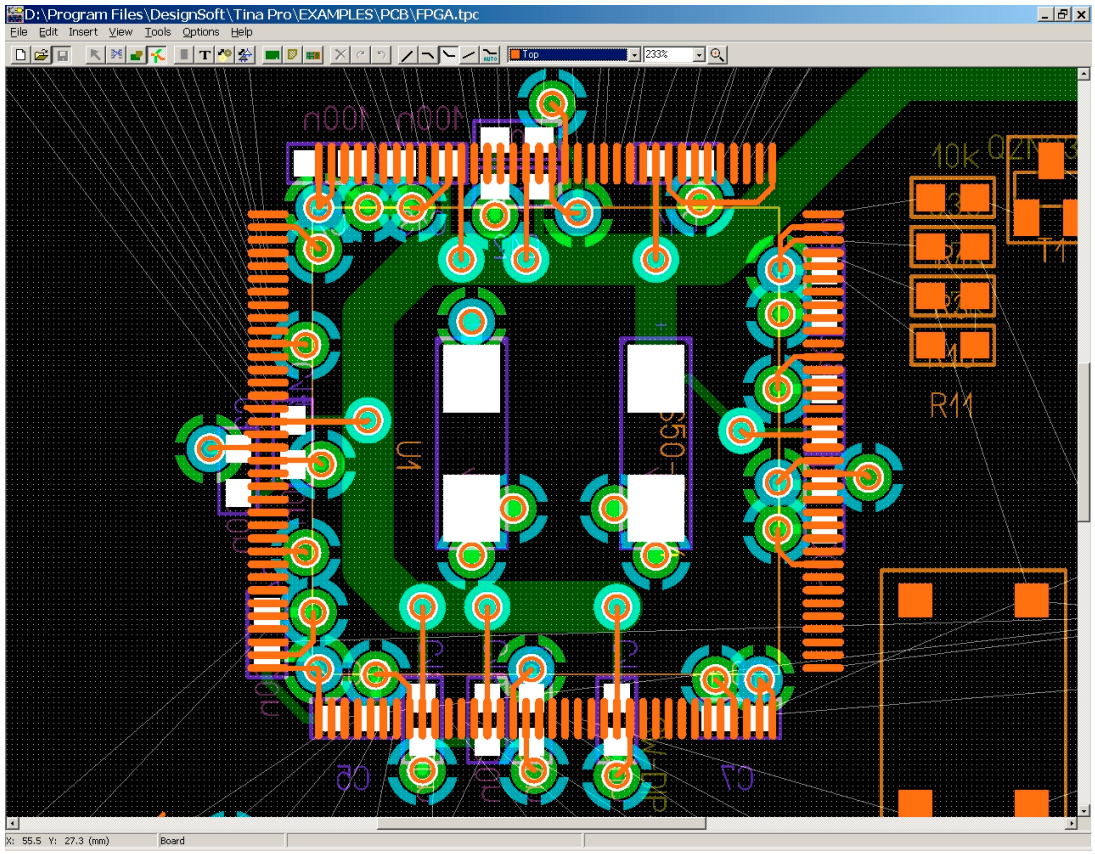
As we have already used two plane layers and still have one more voltage net to route–the 2.5V regulator output going from U4 to the FPGA core–we need a dedicated trace for the 2.5V net. This net touches only a few pins, so we could route a trace to connect all the components. Click on the Draw tracks tool and route 2.5V under the Xilinx chip package onto the bottom side.

---

1 Fanout is the process of routing a SMD pad to a via so that the pad can be routed on other layers. For power and ground pads, the fanout is attached to a power or ground plane using a thermal relief.



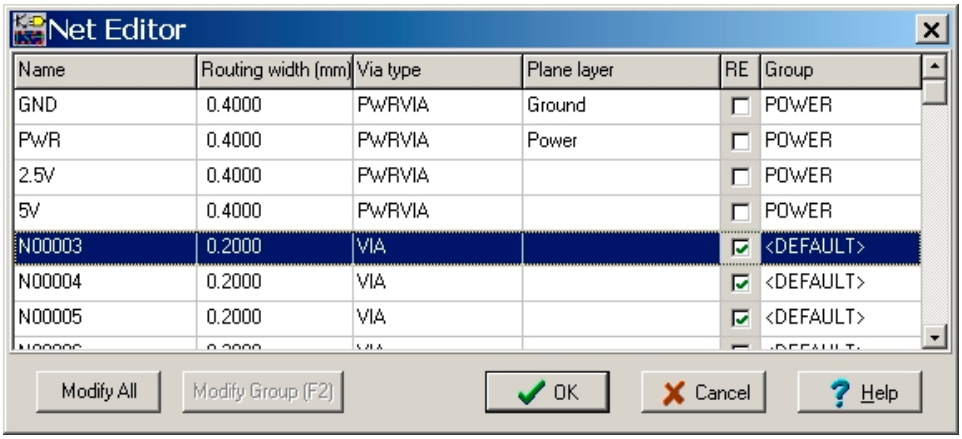
Connect all the power pins of the FPGA, then the pads of filter and decoupling capacitors; set the track width to 0.4mm. Now make the power track 2mm wide as shown below by double clicking on the track.



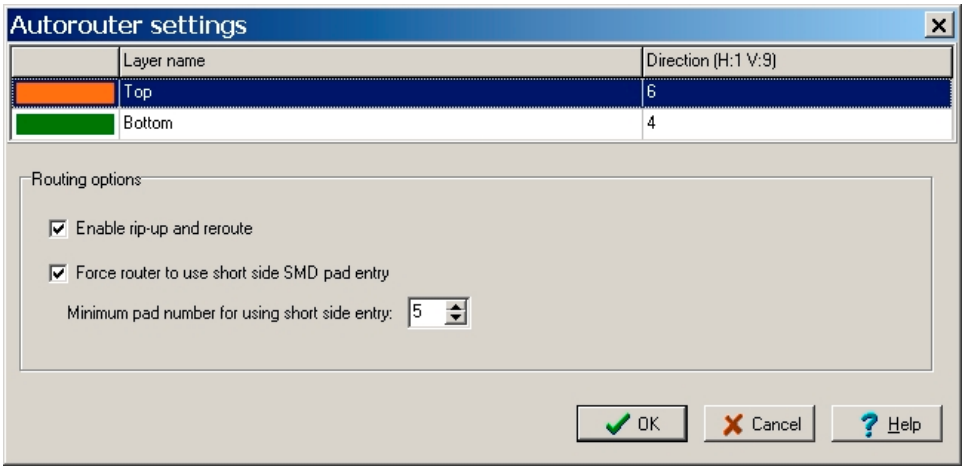
Next, route all the nets from the POWER net group. When you are manually routing, you can begin/end a new track on another track of the same net, which is known as T-routing. After all that press F7 to run DRC. You will not see any unrouted nets belonging to this group (a good thing!).(See FPGA power routed.tpc as reference.)

4.4 Finishing the routing and post processing

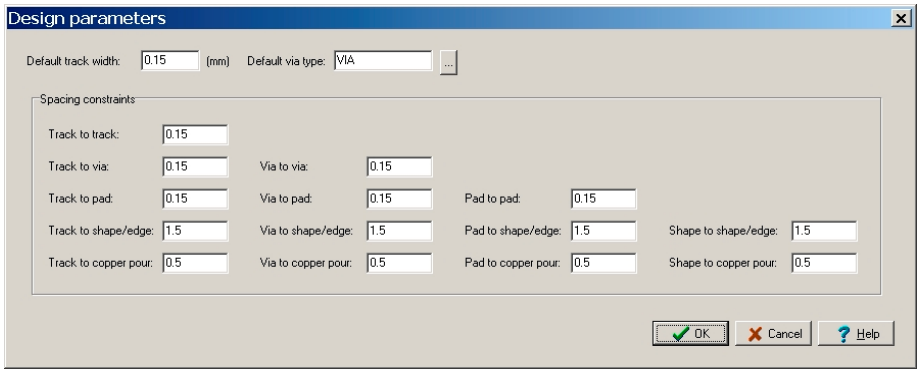
Disable routing on the POWER net group and enable it on the other signals.



Set the autorouter in the Options/Autorouter settings as follows.



Check the settings under Options/Design Parameters.

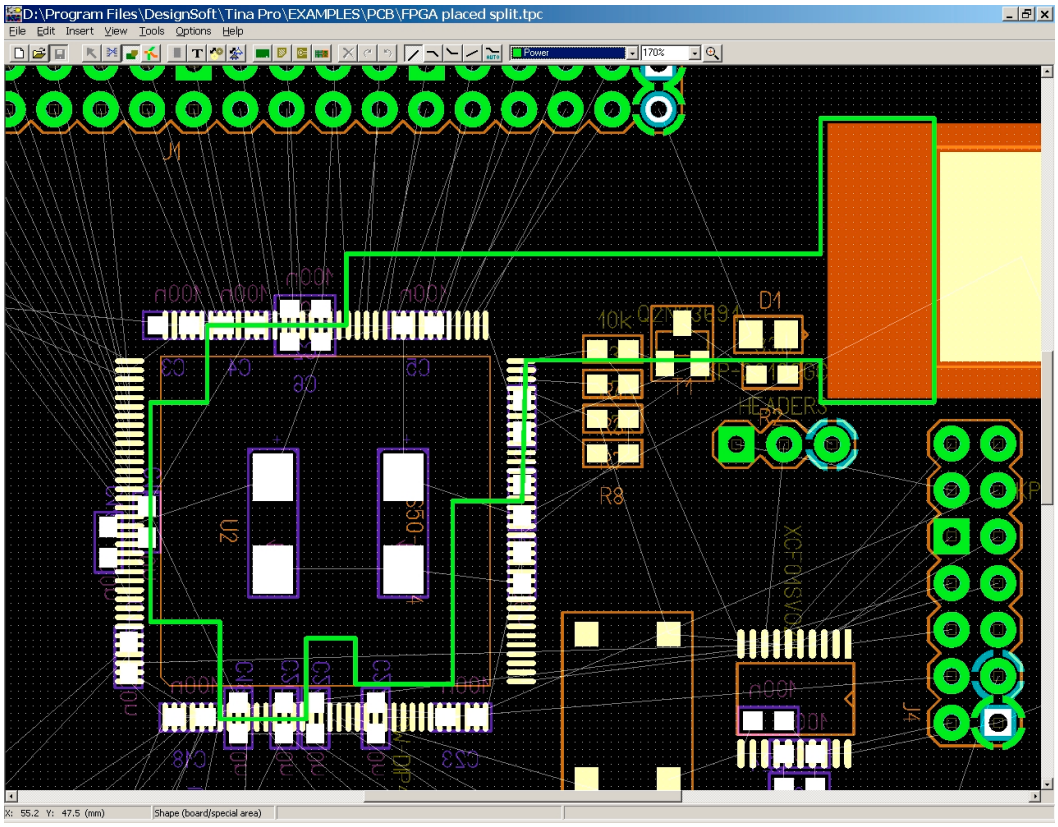


Press F5 to autoroute the whole board, then renumber components (Tools/Renumber components, F10). Renumbering begins at the upper left of the board, renames components in a sweep from left to right, then moves down and renames in successive sweeps.
After renumbering, backannotate the design, as you did in chapter 4.8, and save the new schematic. To check the result, refer to FPGA.TSC and compare.

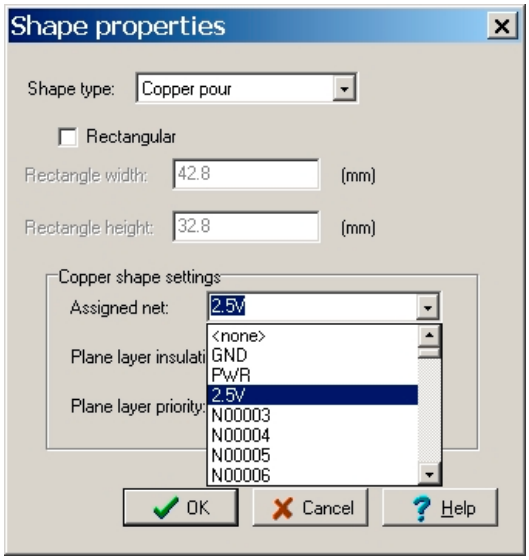
CREATING SPLIT PLANE LAYERS

Power layers are used to provide electrical power references and a stable ground throughout the board. In systems with multiple power supplies, the power planes, which are typically solid copper internal layers, are split. When you split the plane, you assign a part of a plane layer to a second net (e.g.: processor core voltage) by placing a copper pour onto a plane layer. You assign a primary net to the whole plane layer as we did by the GND and PWR IDs in TINA Pro, and a secondary net to the copper pour. Now, let's see how it works within TINA PCB. Open the "FPGA placed.tpc" as a starting point to our work. Remember that the PWR net – the 3.3V primary supply voltage–has already been assigned to the plane layer Power. Now, you split a portion of that plane for the FPGA core voltage (2.5V) instead of routing a net from U4.

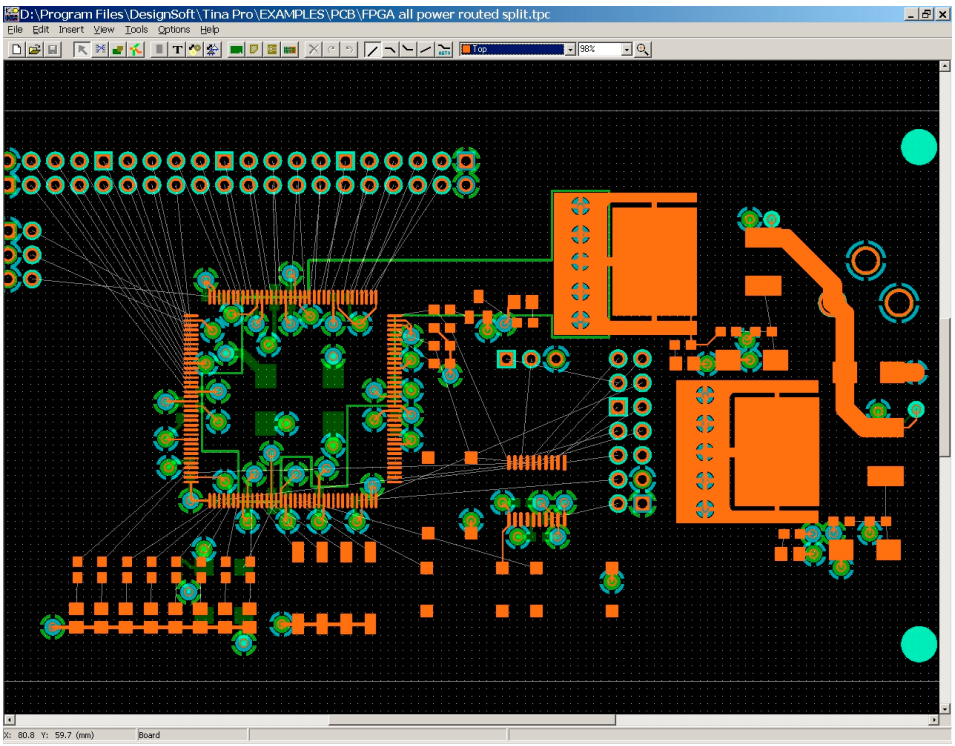
First, it is important to select the power layer, then click the Draw/modify shapes and Add copper pour area buttons. The cursor turns into a cross. You can begin to draw the outline of the copper pour. The shape must extend under the regulator heatsink and the middle of the Xilinx chip package to connect them through vias. Using the appropriate zoom factor (e.g.: 200-400%) during the drawing is usually helpful. When you are done splitting, your design may look something like the screen shot below. (Find this phase of the project in the file "/Examples/PCB/FPGA placed split.tpc".)



Plane layers are negative layers, so only the isolating „moats" can be seen on the screen. Before beginning other tasks, you should assign the 2.5V net to its split area. Double click on the shape, select the 2.5V net, and click OK.



Note that if you create nested copper pours on plane layers which overlap themselves, you must specify the plane layer priority. The higher the priority number, the higher the copper pour sits above the lower ones owning the overlapping region.
If you now establish all the power connections, you will achieve a result similar to "FPGA all power routed split.tpc" shown below. The PCB Designer automatically places thermal reliefs around through-hole pins and vias whenever appropriate.



The rest of the process and the movements are similar to those which we applied in the example with the unpartitioned plane layers.

CONTENTS

CREATING A PRINTED CIRCUIT BOARD 3

1.1 Setting and checking footprint names 3

1.2 Invoking TINA PCB 7

1.3 Advanced editing functions of TINA PCB's Layout Editor.....12

CREATING A TWO-LAYER, DOUBLE-SIDED, SURFACE-MOUNT TECHNOLOGY BOARD.....13

CREATING PCB COMPONENTS.....23

CREATING 4 LAYER PCB LAYOUT.....27

4.1 Placing parts.....29

4.2 Draw copper areas for voltage regulators.....31

4.3 Assigning and routing Ground and Power 33

4.4 Finishing the routing and post processing 37

CREATING SPLIT PLANE LAYERS 39